Service Manual

Tektronix

Tektronix Logic Analyzer Module (TLA7Nx, LTA7Px, & TLA7Qx)

071-0864-01

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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WARRANTY

Tektronix warrants that the products that it manufactures and sells will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If a product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; c) to repair any damage or malfunction caused by the use of non-Tektronix supplies; or d) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the instrument.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Connect the ground lead of the probe to earth ground only.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Replace Batteries Properly. Replace batteries only with the proper type and rating specified.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This is the service manual for the TLA7Nx/7Px/7Qx Logic Analyzer Module. Read this preface to learn how this manual is structured, what conventions it uses, and where you can find other information related to servicing this product. Read the Introduction, which follows this preface, for important background information needed before using this manual for servicing this product.

Manual Structure

The *Logic Analyzer Module (TLA7Nx/7Px/7Qx) Service Manual* is divided into chapters, which are made up of related subordinate topics. These topics can be cross referenced as sections.

Be sure to read the introductions in the sections and subsections because they contain information that you will need to do the service correctly and efficiently.

A brief description of each chapter follows:

- *Specifications* contains a product description of the logic analyzer module and tables of the characteristics and descriptions that apply to it.
- *Operating Information* includes basic installation and operating instructions at the level needed to safely operate and service the logic analyzer module. For complete installation and configuration procedures, refer to the *Tektronix Logic Analyzer Family User Manual*.
- *Theory of Operation* contains circuit descriptions that support general service to the circuit board level.
- *Performance Verification* contains the performance verification procedures for the logic analyzer module, logic analyzer module probes, and the adjustment/verification fixture.
- *Adjustment Procedures* contains the adjustment procedures for the logic analyzer module and the adjustment/verification fixture.
- *Maintenance* contains information and procedures for doing preventive and corrective maintenance on the logic analyzer module. Included are instructions for cleaning, for removal and installation of replacement parts, and for troubleshooting to the circuit board level.
- *Options* contains information on servicing any of the factory-installed options that may be available for the logic analyzer module.

- *Diagrams* contains block diagrams and interconnection diagrams that are useful when isolating failed circuit boards.
- *Mechanical Parts List* includes a table of all replaceable parts, their descriptions, and their Tektronix part numbers.

Manual Conventions

This manual uses certain conventions that you should be familiar with before attempting service.

Acquisition Board The acquisition board is one of the circuit boards inside the logic analyzer module. The circuit board receives and stores acquisition data from the probes and works with the LPU board to provide logic analysis information to the operator of the logic analyzer.

Adjustment Procedures Adjustment procedures check for, and if necessary, correct any adjustment errors discovered when performing functional or performance verification procedures.

Adjustment/Verification Fixture The adjustment/verification fixture is a test fixture used to perform the adjustment, functional check, and performance verification procedures. Specifications and replaceable parts information are documented in this service manual.

Certification Procedures Certification procedures certify a product and provide a traceability path to national standards.

Daughter Board The daughter board provides additional channels for the logic analyzer. Data from these channels is sent to the acquisition board for processing with other data from the acquisition board.

Functional Verification Procedures Functional verification procedures verify the basic functionality of the instrument. These procedures include power-on and extended diagnostics, self calibration, as well as semi-automated or manual check procedures. These procedures can be used as incoming inspection purposes. This manual provides information on power-on and extended diagnostics and the self calibration.

LPU Board The Local Processor Unit (LPU) Board. The LPU board is one of the circuit boards inside the logic analyzer module that provides the main communications interface with the mainframe.

Maintenance Procedures Maintenance procedures are used for fault isolation and repair to the circuit board level or to the replaceable part level.

Modules Throughout this manual, the term "module" refers to a logic analyzer or DSO unit that mounts inside a mainframe. A module is composed of circuit cards, interconnecting cables, and a user-accessible front panel.

Performance Verification Procedures Performance verification procedures confirm that a product meets or exceeds the performance requirements for each of the published specifications.

Replaceable Parts This manual refers to any field-replaceable assembly or mechanical part specifically by its name or generically as a replaceable part. In general, a replaceable part is any circuit board or assembly, such as the hard disk drive, or a mechanical part, such as the I/O port connectors, that is listed in the replaceable parts list.

Safety Symbols and terms related to safety appear in the *Safety Summary* found at the beginning of this manual.

Related Manuals

The following manuals are available as part of the TLA700 Series Logic Analyzer documentation set. Refer to *Optional Accessories* on page 10–7 for part numbers.

Manual Name	Description	Service use
Tektronix Logic Analyzer Family User Manual	Provides operating information on the TLA Series Logic Analyzer	Augments operating information found in chapter 2 of this manual
TLA715 Portable Mainframe Service Manual	Provides service information for the portable mainframes	Isolating and correcting failures in the portable mainframe
TLA721 Benchtop Mainframe and TLA7XM Expansion Mainframe Service Manual	Provides service information for the benchtop mainframe and expansion mainframe	Isolating and correcting failures in the benchtop mainframe, controller, or expansion mainframe
TLA7Dx/TLA7Ex Digitizing Oscilloscope Service Manual	Provides service information for the digitizing oscilloscope modules	Isolating and correcting failures in the DSO module

Contacting Tektronix

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*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Introduction

This manual contains information needed to properly service the logic analyzer module, as well as general information critical to safe servicing.

To prevent personal injury or damage consider the following requirements before attempting service:

- The procedures in this manual should be performed only by a qualified service person.
- Read the *General Safety Summary* and *Service Safety Summary* found at the beginning of this manual.

When using this manual for servicing follow all warnings and cautions.

Adjustment and Certification Interval

Generally, you should perform the adjustments and certification (calibration) described in the *Performance Verification* and *Adjustment Procedures* chapters once per year, or following repairs that affect adjustment or calibration.

Strategy for Servicing

This manual contains information for corrective maintenance of this product:

- Supports isolation of faults to the failed circuit board or assembly level shown in the replaceable parts list
- Supports removal and replacement of those boards or assemblies
- Supports removal and replacement of fuses, knobs, chassis, and other mechanical parts listed in the replaceable parts list

This manual does not support component-level fault isolation and replacement.

Service Offerings

Tektronix provides service to cover repair under warranty as well as other services that are designed to meet your specific service needs.

Whether providing warranty repair service or any of the other services listed below, Tektronix service technicians are well equipped to service the logic analyzer module.

Warranty Repair Service

Tektronix warrants this product for one year from date of purchase. (The warranty appears behind the title page in this manual.) Tektronix technicians provide warranty service at most Tektronix service locations worldwide. The Tektronix product catalog lists all service locations worldwide or you can visit us on our *Customer Services World Center* web site at http://www.tek.com/Measurement/Service. See our latest service offerings and contact us by email.

Calibration and Repair Service

In addition to warranty repair, Tektronix Service offers calibration and other services that provide cost-effective solutions to your service needs and quality-standards compliance requirements. Our instruments are supported worldwide by the leading-edge design, manufacturing, and service resources of Tektronix to provide the best possible service.

The following services can be tailored to fit your requirements for calibration and/or repair of the logic analyzer module.

Service Options

Tektronix Service Options can be selected at the time you purchase your instrument. You select these options to provide the services that best meet your service needs.

Service Agreements

If service options are not added to the instrument purchase, then service agreements are available on an annual basis to provide calibration services or post-warranty repair coverage for the logic analyzer module. Service agreements may be customized to meet special turn-around time and/or on-site requirements.

Service On Demand

Tektronix also offers calibration and repair services on a “per-incident” basis that is available with standard prices for many products.

Self Service

Tektronix supports repair to the replaceable-part level by providing for circuit board exchange. Use this service to reduce down-time for repair by exchanging circuit boards for remanufactured ones. Tektronix ships updated and tested exchange boards. Each board comes with a 90-day service warranty.

When you exchange circuit boards, you must supply the following information to allow the board to be preconfigured to the proper PowerFlex level. You can also return the repaired module to your local service center for configuration.

- Model number and serial number
- PowerFlex option upgrade number
- Firmware level

For More Information

Contact your local Tektronix service center or sales engineer for more information on any of the Calibration and Repair Services just described.

Specifications

This chapter provides a brief product description, specifications and characteristics of the logic analyzer module and the adjustmernt/verification fixture.

Product Description

The logic analyzer module is designed to be used with either the benchtop mainframe or portable mainframe in a TLA700 Series Logic Analyzer. The logic analyzer module is used as a test and measurement tool for high-speed digital timing and state acquisition across several channels.

Some of the key features of the logic analyzer module include the following:

- 100 MHz synchronous acquisition with a programmable setup and hold window (PowerFlex configurable to 200 MHz)
- 250 MHz asynchronous full depth selections with selectable sampling rates
- 2 GHz asynchronous acquisition into a 2 K high resolution timing buffer
- 250 MHz trigger capability, plus special setup and hold violation triggering and glitch triggering
- Data correlation with other modules

Characteristic Tables

This section lists the specifications for the logic analyzer module. All specifications are guaranteed unless noted *Typical*. Specifications that are marked with the ✓ symbol are checked directly (or indirectly) in the *Performance Verification* chapter. The specifications apply to all versions of the logic analyzer module unless otherwise noted.

The performance limits in this specification are valid with these conditions:

- The logic analyzer module must have been calibrated/adjusted at an ambient temperature between +20° C and +30° C.
- The logic analyzer module must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The logic analyzer module must have had a warm-up period of at least 30 minutes.

- The logic analyzer module must have had its signal-path-compensation routine (self-calibration) last executed after at least a 30 minute warm-up period.

Table 1-1: LA module channel width and depth

Characteristic	Description	
Number of channels	Product	Channels
	TLA7N1	32 data and 2 clock
	TLA7N2, TLA7P2, TLA7Q2	64 data and 4 clock
	TLA7N3, TLA7L3, TLA7M3	96 data, 4 clock, and 2 qualifier
	TLA7N4, TLA7P4, TLA7Q4	128 data, 4 clock, and 4 qualifier
Acquisition memory depth	Product	Memory depth
	TLA7L1, TLA7L2, TLA7L3, TLA7L4	32 K or 128 K samples
	TLA7N1, TLA7N2, TLA7N3, TLA7N4	64 K or 256 K or 1 M or 4 M samples[1]
	TLA7P2, TLA7P4	16 M samples
	TLA7Q2, TLAQP4	64 M samples

[1] **PowerFlex options**

Table 1-2: LA module clocking

Characteristic	Description	
Asynchronous clocking		
✓ Internal sampling period[1]	4 ns to 50 ms in a 1-2-5 sequence 2 ns in 2x Clocking mode	
✓ Minimum recognizable word[2] (across all channels)	Channel-to-channel skew + sample uncertainty Example: for a P6417 or a P6418 Probe and a 4 ns sample period = 1.6 ns + 4 ns = 5.6 ns	
Synchronous clocking		
Number of clock channels[3]	Product	Clock channels
	TLA7N1	2
	TLA7N2, TLA7P2, TLA7Q2	4
	TLA7N3	4
	TLA7N4, TLA7P4, TLA7Q4	4
Number of qualifier channels	Product	Qualifier channels
	TLA7N1	0
	TLA7N2, TLA7P2, TLA7Q2	0
	TLA7N3	2

Table 1-2: LA module clocking (Cont.)

Characteristic	Description
	TLA7N4, TLA7P4, TLA7Q4 | 4
✓ Setup and hold window size (data and qualifiers)	Maximum window size = Maximum channel-to-channel skew + (2 x sample uncertainty) + 0.4 ns Maximum setup time = User interface setup time + 0.8 ns Maximum hold time = User interface hold time + 0.2 ns Maximum setup time for slave module of merged pair = User Interface setup time + 0.8 ns Maximum hold time for slave module of merged pair = User Interface hold time + 0.7 ns Examples: for a P6417 or a P6418 probe and user interface setup and hold of 2.0/0.0 typical: Maximum window size = 1.6 ns + (2 x 500 ps) + 0.4ns = 3.0 ns Maximum setup time = 2.0 ns + 0.8 ns = 2.8 ns Maximum hold time = 0.0 ns + 0.2 ns = 0.2ns
Setup and hold window size (data and qualifiers) (Typical)	Channel-to-channel skew (*typical*) + (2 x sample uncertainty) Example: for P6417 or P6418 Probe = 1 ns + (2 x 500 ps) = 2 ns
Setup and hold window range	The setup and hold window can be moved for each channel group from +8.5 ns (Ts) to -7.0 ns (Ts) in 0.5 ns steps (setup time). Hold time follows the setup time by the setup and hold window size.
✓ Maximum synchronous clock rate[4]	200 MHz in full speed mode (5 ns minimum between active clock edges) 100 MHz in half speed mode (10 ns minimum between active clock edges)
Demux clocking	
Demux Channels TLA7N3, TLA7N4, TLA7P4, TLA7Q4,	Channels multiplex as follows: A3(7:0) to D3(7:0) A2(7:0) to D2(7:0) A1(7:0) to D1(7:0) A0(7:0) to D0(7:0)
TLA7N1, TLA7N2, TLA7P2, TLA7Q2	Channels multiplex as follows: A3(7:0) to C3(7:0) A2(7:0) to C2(7:0) A1(7:0) to D1(7:0) TLA7N2, TLA7P2, TLA7Q2 only A0(7:0) to D0(7:0) TLA7N2, TLA7P2, TLA7Q2 only
Time between DeMux clock edges[4] (Typical)	5 ns minimum between DeMux clock edges in full-speed mode 10 ns minimum between DeMux clock edges in half-speed mode
Time between DeMux store clock edges[4] (Typical)	10 ns minimum between DeMux master clock edges in full-speed mode 20 ns minimum between DeMux master clock edges in half-speed mode
Data Rate (Typical) TLA7N1, TLA7N2, TLA7P2, TLA7Q2, TLA7N3, TLA7N4, TLA7P4, TLA7Q4,	400 MHz (200 MHz option required) half channel. (Requires channels to be multiplexed.) These multiplexed channels double the memory depth.

Table 1-2: LA module clocking (Cont.)

Characteristic	Description
Clocking state machine	
Pipeline delays	Each channel group can be programmed with a pipeline delay of 0 through 3 active clock edges.

1 It is possible to use storage control and only store data when it has changed (transitional storage).

2 Applies to asynchronous clocking only. Setup and hold window specification applies to synchronous clocking only.

3 Any or all of the clock channels may be enabled. For an enabled clock channel, either the rising, falling, or both edges can be selected as the active clock edges. The clock channels are stored.

4 Full and half speed modes are controlled by PowerFlex options and upgrade kits.

Table 1-3: LA module trigger system

Characteristic	Description
Triggering resources	
Word/Range recognizers	16 word recognizers. The word recognizers can be combined to form full width, double bounded, range recognizers. The following selections are available: 16 word recognizers — 0 range recognizers 13 word recognizers — 1 range recognizer 10 word recognizers — 2 range recognizers 7 word recognizers — 3 range recognizers 4 word recognizers — 4 range recognizers
Range recognizer channel order	From most-significant probe group to least-significant probe group: C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0 Missing channels for modules with fewer than 136 channels are omitted. When merged, the range recognition extends across all the modules; the master module contains the most-significant groups. The master module is to the left (lower-numbered slot) of a merged pair. The master module is in the center when three modules are merged. Slave module 1 is located to the right of the master module, and slave module 2 is located to the left of the master module.
Glitch detector[1,2]	Each channel group can be enabled to detect a glitch
Minimum detectable glitch pulse width (Typical)	2.0 ns (single channel with P6417 or a P6418 probe)
Setup and hold violation detector[1,3]	Each channel group can be enabled to detect a setup and hold violation. The range is from 8 ns before the clock edge to 8 ns after the clock edge. The range can be selected in 0.5 ns increments. The setup and hold violation of each window can be individually programmed.
Transition detector[1, 4]	Each channel group can be enabled or disabled to detect a transition between the current valid data sample and the previous valid data sample.

Table 1-3: LA module trigger system (Cont.)

Characteristic	Description
Counter/Timers	2 counter/timers, 51 bits wide, can be clocked up to 250 MHz. Maximum count is 2^{51}. Maximum time is 9.007×10^6 seconds or 104 days. Counters and timers can be set, reset, or tested and have zero reset latency.
Signal In 1	A backplane input signal
Signal In 2	A backplane input signal
Trigger In	A backplane input signal that causes the main acquisition and the MagniVu acquisition to trigger if they are not already triggered
Active trigger resources	16 maximum (excluding counter/timers) Word recognizers are traded off one-by-one as Signal In 1, Signal In 2, glitch detection, setup and hold detection, or transition detection resources are added.
Trigger States	16
✓ Trigger State sequence rate	Same rate as valid data samples received, 250 MHz maximum
Trigger Machine Actions	
Main acquisition trigger	Triggers the main acquisition memory
Main trigger position	Trigger position is programmable to any data sample (4 ns boundaries)
Increment counter	Either of the two counter/timers used as counters can be incremented.
Start/Stop timer	Either of the two counter/timers used as timers can be started or stopped.
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer is used as a timer and is reset, the timer continues in the started or stopped state that it was in prior to the reset.
Signal out	A signal sent to the backplane to be used by other modules
Trigger out	A trigger out signal sent to the backplane to trigger other modules

Table 1-3: LA module trigger system (Cont.)

Characteristic	Description
Storage control	
Global storage	Storage is allowed only when a specific condition is met. This condition can use any of the trigger machine resources except for the counter/timers. Storage commands defined in the current trigger state will override the global storage control. Global storage can be used to start the acquisition with storage initially turned on (default) or turned off.
By event	Storage can be turned on or off; only the current sample can be stored. The event storage control overrides any global storage commands.
Block storage	When enabled, 31 samples are stored before and after the valid sample. Block storage is disallowed when glitch storage or setup and hold violation is enabled.
Glitch violation storage	The acquisition memory can be enabled to store glitch violation information with each data sample when asynchronous clocking is used. The probe data storage size is reduced by one half (the other half holds the violation information). The fastest asynchronous clocking rate is reduced to 10 ns.

[1] Each use of a glitch detector, setup and hold violation detector, or transition detector requires a trade-off of one word recognizer resource.

[2] Any glitch is subject to pulse width variation of up to the channel-to-channel skew specification + 0.5 ns.

[3] For TLA7N1, TLA7N2, TLA7N3, TLA7N4, TLA7P2, TLA7P4, TLA7Q2, and TLA7Q4 Logic Analyzer modules, any setup value is subject to variation of up to 1.8 ns; any hold value is subject to variation of up to 1.2 ns.

[4] This mode can be used to create transitional storage selections where all channels are enabled.

Table 1-4: LA module MagniVu feature

Characteristic	Description
MagniVu memory depth	2016 samples per channel
MagniVu sampling period	Data is asynchronously sampled and stored every 500 ps in a separate high resolution memory.

Table 1-5: LA module data handling

Characteristic	Description
Nonvolatile memory retention time (Typical)	Battery is integral to the NVRAM. Battery life is > 10 years.

Table 1-6: LA module input parameters with probes

Characteristic	Description
✓ Threshold Accuracy	±100 mV
Threshold range and step size	Setable from +5 V to -2 V in 50 mV steps
Threshold channel selection	16 threshold groups assigned to channels. P6417 and P6418 probes have two threshold settings, one for the clock/qualifier channel and one for the data channels. P6434 probes have four threshold settings, one for each of the clock/qualifier channels and two for the data channels (one per 16 data channels).
✓ Channel-to-channel skew	≤ 1.6 ns maximum (When merged, add 0.5 ns for the slave module.)
Channel-to-channel skew (Typical)	≤ 1.0 ns typical (When merged, add 0.3 ns for the slave module.)
Sample uncertainty	
Asynchronous:	Sample period
Synchronous:	500 ps
Probe input resistance (Typical)	20 kΩ
Probe input capacitance: P6417, P6434 (Typical)	2 pF
Probe input capacitance: P6418 (Typical)	1.4 pF data channels 2 pF CLK/Qual channels
Minimum slew rate (Typical)	0.2 V/ns
Maximum operating signal	6.5 V_{p-p} -3.5 V absolute input voltage minimum 6.5 V absolute input voltage maximum
Probe overdrive: P6417, P6418 P6434	 ±250 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater ±300 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater ±4 V maximum beyond threshold
Maximum nondestructive input signal to probe	±15 V
Minimum input pulse width signal (single channel) (Typical)	2 ns
Delay time from probe tip to input probe connector (Typical)	7.33 ns

Table 1-7: LA module mechanical

Characteristic	Description
Slot width	Requires 2 mainframe slots
Weight (Typical)	5 lbs 10 oz. (2.55 kg) for TLA7N4, TLA7P4 or TLA7Q4 8 lbs (3.63 kg) for TLA7N4, TLA7P4 or TLA7Q4 packaged for domestic shipping
Overall dimensions	
Height	262 mm (10.32 in)
Width	61 mm (2.39 in)
Depth	373 mm (14.7 in)
Probe cables	
P6417 length	1.8 m (6 ft)
P6418 length	1.93 m (6 ft 4 in)
P6434 length	1.6 m (5 ft 2 in)
Mainframe interlock	1.4 ECL keying is implemented

Table 1-8: Merged modules

Characteristic	Description
Number of modules that can be merged together	Refer to *Merging Rules* on page 2-10.
Number channels after merge	The sum of the data channels of both modules plus the CLK/QUAL channels (active clocks for the merge system) of the master module plus the CLK/QUAL channels (nonactive stored clock channels to the merge system).
Merge system acquisition depth	Channel depth is equal to the smallest depth of the modules.
Number of clock and qualifier channels after merge	Same number of clock and qualifier channels on the master module. The clock and qualifier channels on the slave module have no effect on clocking and are only stored.
Merge system triggering resources	Triggering resources are the same as a single module except that the widths of the word/range recognizers, setup and hold violation detector, glitch detector, and transition detector are increased to the merged channel width.

Table 1-9: Atmospherics

Characteristic	Description
Altitude	
Operating	To 10,000 ft. (3040 m) (derated 1° C per 1000 ft (305 m) above 5000 ft (1524 m) altitude)
Non-operating	40,000 ft. (12190 m)
Temperature	

Table 1-9: Atmospherics (Cont.)

Characteristic	Description
Operating	+5° C to +50° C, 15° C/hour maximum gradient, non-condensing (derated 1° C/1000 ft. above 5000 ft altitude)
Non-operating	-20° to +60° C, 15° C/hour maximum gradient, non-condensing
Relative Humidity	
Operating and non-operating	20% to 80% relative humidity, non-condensing. Maximum wet bulb temperature: +29° C (derates relative humidity to approximately 22% at +50° C)
Non-operating	8% to 80% relative humidity, non-condensing. Maximum wet bulb temperature: +29° C (derates relative humidity to approximately 22% at +50° C)

Table 1-10: Certifications and compliances

EC Declaration of Conformity - EMC	Meets intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities: EN 55011 Class A Radiated and Conducted Emissions EN 50081-1 Emissions: EN 60555-2 AC Power Line Harmonic Emissions EN 50082-1 Immunity: IEC 801-2 Electrostatic Discharge Immunity IEC 801-3 RF Electromagnetic Field Immunity IEC 801-4 Electrical Fast Transient/Burst Immunity IEC 801-5 Power Line Surge Immunity

Table 1-11: Adjustment/verification fixture specifications

Characteristic	Description
Instrument characteristics	
Number of data outputs	
For P6417 Probes	18 grouped in two groups of eight and one group of two
For P6418 Probes	18 grouped in two groups of eight and one group of two
For P6434 Probes	36 grouped in one connector
Number of setup and hold clock outputs	
For P6417 Probes	Two grouped in one group of two
For P6418 Probes	Two grouped in one group of two
For P6434 Probes	One clock
Number of DC threshold outputs	
For P6417 Probes	16 grouped in two groups of eight and one group of two

Table 1-11: Adjustment/verification fixture specifications (Cont.)

Characteristic	Description
For P6418 Probes	16 grouped in two groups of eight and one group of two
For P6434 Probes	36 grouped in one connector
External clock in	External clock input provided by user through a BNC connector
DC threshold input	External input provided by user through a BNC connector
DC power in	Provided by a wall transformer DC power supply (9 V to 12 V DC)
V_{DD} DC level (*typical)*	+5 V referenced to V_{EE}
V_{DD} to analog ground level (*typical)*	+2 V referenced to ground (GND)
V_{DD} switcher noise (*typical)*	50 mV_{p-p} (measured at C17)
✓ Internal clock frequency	50.065 MHz ±0.01%
Output electrical characteristics	
Data/clock output amplitude	10K Motorola ECLinPS family outputs
DC threshold output	Output equals user-applied input
Input requirements	
External Clock input	1.0 V_{p-p} centered around the fixture ground. Specification is valid between 5 MHz and 210 MHz
DC power in	12 Volts DC at 1.5 A. Power is provided by one of the following power supply wall plugs: 119-4855-00, 119-4856-00, 119-4859-00, and 119-4857-00
DC threshold input	Input not greater than ±5 V ground referenced
Output timing	
✓ Data output (channel-to-channel skew)	50 ps (all channels within 50 ps relative to each other)
✓ Setup clock output timing	Adjusted for +3.0 ns (setup) ±100 ps, referenced to one of the data outputs
✓ Hold clock output timing	Adjusted for 0.0 ns (hold) ±100 ps, referenced to one of the data outputs
Minimum data output pulse width	Adjusted for 2.0 ns ±100 ps (jumpered in minimum pulse width mode)
Fuse rating	
Recommended replacement fuse	1.5 AF, 125 V, Tektronix part number 159-5009-00

Operating Information

This chapter provides brief operating information for performing maintenance. The operating information is limited to the functions you need to perform the procedures found in this document. You can find more detailed operating instructions in the *Tektronix Logic Analyzer Family User Manual* and in the online help.

Installation

This section contains brief installation information and is provided for your convenience. For detailed installation information, refer to the *Tektronix Logic Analyzer Family User Manual*.

***NOTE**. Do not set the logic analyzer module logical address to 00. Logical address 00 is reserved for the controller.*

Dynamic Autoconfiguration With Dynamic Auto Configuration (Recommended) selected (hexadecimal FF or decimal 255), the logic analyzer automatically sets the address to an unused value. For example, if there are modules set to addresses 01 and 02 already in your system, the resource manager will automatically assign the logic analyzer module an address other than 01 or 02.

Static Logical Address Static logical address selections set the address to a fixed value. A static logical address ensures that the logic analyzer module address remains fixed for compatibility with modules that require a specific address value. Remember that each module within the logic analyzer must have a unique address to avoid communication problems.

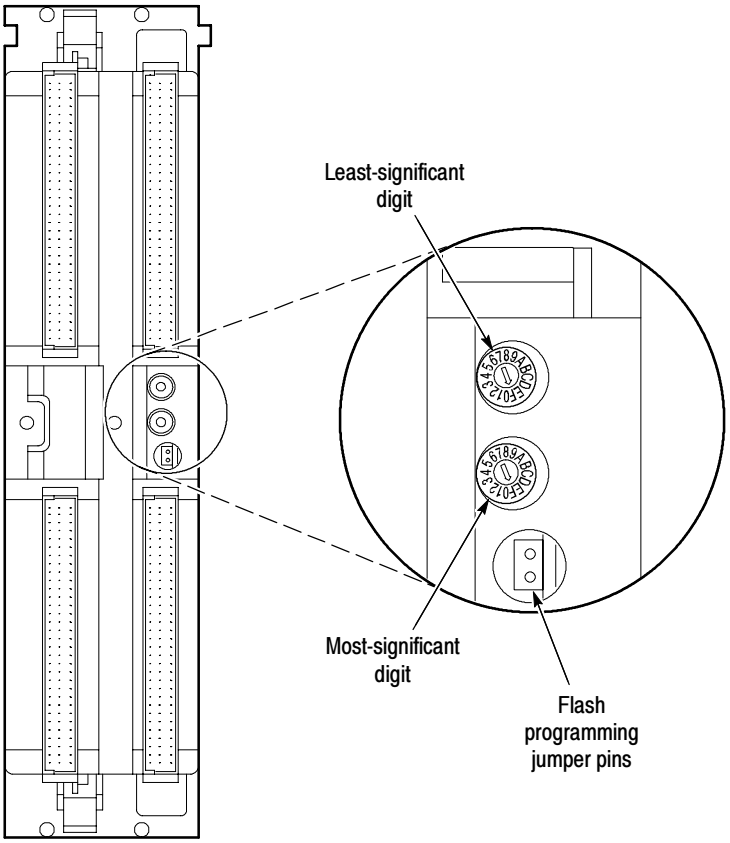


Figure 2- 1: Logical address switches

Merging Modules You can combine up to three logic analyzer modules to create a single two- or three-wide module. This process is called merging modules. The procedures for merging modules is described in the *Tektronix Logic Analyzer Family User Manual*.

Software Installation and Removal

These procedures describe loading and unloading the performance verification and adjustment software. Refer to the *Tektronix Logic Analyzer Family User Manual* for information on installing or removing any other software. It is recommended you have ≥10 MB of free space on the hard drive before installing the software. The Performance Verification software is located on Disk 1 of the Tektronix Logic Analyzer Family Application Software CD.

***NOTE**. This installation program uses parameters you supply to create a custom start-up file in your hard disk directory.*

The batch file enables the software to configure your instrument properly before it runs the program.

1. Power on the instrument.
2. Exit the Application.

Verify PV/Adjust Software Version

If your logic analyzer already has PV/Adjust software loaded on it, you must verify that the version is the same as the version printed on Disc 1 of the Tektronix Logic Analyzer Family Application Software CD.

If the version of the PV/Adjust software loaded on your logic analyzer is an earlier version, you must delete the earlier version before you can load the newer version.

Verify Directories

If your logic analyzer already has a directory named Tekcats or Temptek on the hard drive, the software installation cannot be completed. Follow these instructions to verify the directory is not present:

1. Select Start → Search → For Files or Folders.
2. In the "Search for files or folders:" box, type "Tekcats" or "TempTek" and then click the Search Now button fo search for either directory.
3. If either directory is found follow the instructions under *Removing the Software* to remove the software and the directories.

Install the PV/Adjust Software

Follow these instructions to install the PV/Adjust software.

1. Close all open windows on the desktop.
2. Insert Disk 1 of the Tektronix Logic Analyzer Family Application Software CD in the CD-ROM drive.
3. Click the My Computer Icon and double-click the CD-ROM drive.
4. Double-click the TLA Performance Verification folder.
5. Double-click on the Logic Analyzer PV folder and then double-click the Disk1 folder.
6. Double-click the Setup.exe icon to begin the installation program.
7. Follow the on-screen instructions to install the software on the hard disk.

8. After the installation is complete, go back to the TLA Performance Verification folder on the CD.

This completes the software installation procedure.

Removing the Software

Use the following procedure to remove the performance verification and adjustment software from the instrument. These steps are necessary when you want to upgrade the PV software.

1. Open Windows Explorer and then locate and select the C:\Tekcats folder.
2. Go to the File menu and select Delete to delete the folder.
3. Repeat steps 1 and 2 to find and delete the Temptek folder if it exists.
4. Select Start → Settings → Taskbar & Start Menu.
5. Click the Advanced tab followed by the Advanced button.
6. Open the following directory path under Documents and Settings:

   All Users → Start Menu → Programs
7. Locate and delete the TLA Performance Verification item.

Operating Information

This section provides a general description of the logic analyzer module.

Front Panel

Figure 2–2 on page 2–5 shows the connectors and indicators on the front panel of a 136 channel logic analyzer module. The 102, 68, and 34 channel versions look and operate the same, but without the additional probe connectors.

Injector/Ejector Handles. The injector/ejector tabs are used to seat and unseat the modules in the mainframe.

Probe Connectors. The probe connectors are color-coded to match the labels on the probes.

Probe Retainer Mounting Holes. The threaded probe retainer mounting holes provide a means of securely holding the probes in place.

Configuration Label. The configuration label indicates the speed and memory depth of the logic analyzer module.

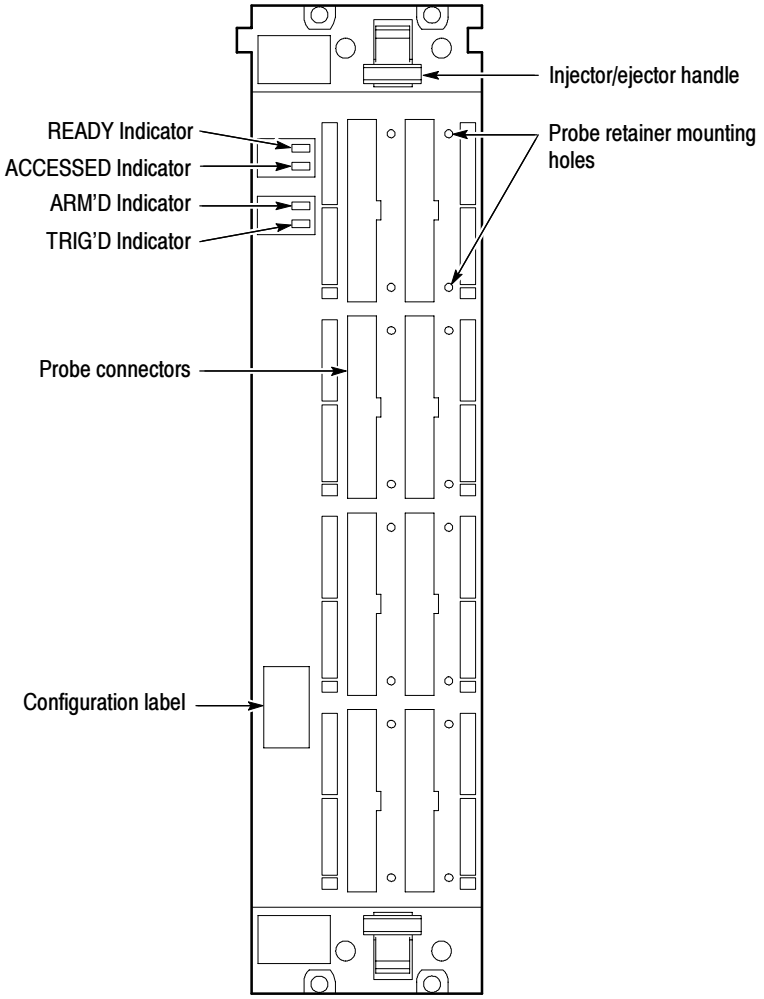


Figure 2-2: Front panel of the logic analyzer module

READY Indicator. The READY indicator lights continuously after the logic analyzer module successfully completes the power-on process. If the indicator fails to light within five seconds of power-on, an internal module failure may be present.

ACCESSED Indicator. The ACCESSED indicator lights anytime the controller accesses the logic analyzer module.

ARM'D Indicator. The ARM'D indicator lights when the logic analyzer module is armed during an acquisition.

TRIG'D Indicator. The TRIG'D indicator lights when the logic analyzer module triggers and stays on until the module finishes acquiring data.

Merge Cable Connectors

The merge cable connectors (not shown) are located on the sides of the logic analyzer module. The connectors are used to merge up to three logic analyzer modules together to create a two- or three-wide logic analyzer module.

Two Merged Modules. When two modules are merged, the master module is on the left (lower numbered slot) and the slave module is on the right.

Three Merged Modules. When three modules are merged, the master module is in the center, and the slave modules are on the right and left of the master module.

Merge Cable Connector. The merge cable connector is located on the side panel of the module. When the module is used by itself the merge cable is stored inside the cover.

When you merge modules together, you must set up the merge connector so that it mates with an adjacent logic analyzer module. Instructions for merging modules are described in the *Tektronix Logic Analyzer Family User Manual*.

Rear Panel

Four rear panel connectors (see Figure 2–1 on page 2–2) connect the logic analyzer module to the backplane of the mainframe. The module receives power, processor communication, and intermodule communication through these four connectors.

Logical Address Switches. Figure 2–1 on page 2–2 shows the location of the logical address switches.

Flash Programming Jumper Pins. Figure 2–1 on page 2–2 shows the location of the two pins that are used when updating the firmware of the logic analyzer module. You must jumper the pins when updating the flash image. The logic analyzer module is shipped without a jumper installed on these pins. Refer to the *Tektronix Logic Analyzer Family User Manual* for instructions on upgrading the firmware.

Online Help

Most user information for operating the logic analyzer module is available through the online help within the Tektronix Logic Analyzer Series application.

Diagnostics

The logic analyzer module performs the power-on diagnostics each time you power on the mainframe. The Calibration and Diagnostics property sheet appears at power-on if one of the module diagnostics fails. You can also access the diagnostics from the System menu. For additional diagnostics information, refer to *Calibration and Diagnostics Procedures*, beginning on page 6–32.

In addition to the power-on diagnostics, you can also run the extended diagnostics or the self calibration.

***NOTE**. For best results, only run the diagnostics with probes disconnected from the module.*

Self Calibration

Self calibration is an internal routine that optimizes performance. No external equipment or user actions are needed to complete the procedure. The logic analyzer module saves data generated by the self calibration in non-volatile memory.

***NOTE**. Performing the self calibration does not guarantee that all logic analyzer module parameters operate within limits. Operation within limits is achieved by performing the* Adjustment Procedures. *Proper operation may be confirmed by performing the performance verification procedures in this same manual.*

When to Perform the Self Calibration. You can run the self calibration at any time during normal operation. To maintain measurement accuracy, perform the self calibration if more than one year has elapsed since the last self calibration.

You can check the status of the self calibration in the Calibration and Diagnostics property sheet.

If the logic analyzer module loses power during the self calibration, rerun the self calibration following the next power-on. The self calibration data generated before power was interrupted must be replaced with a complete set of new data. For best results, always perform the self calibration after at least a 30 minute warm-up.

Running the Self Calibration. The logic analyzer module may require several minutes to run the self calibration depending on the number of channels. Select Calibration and Diagnostics property sheet from the System menu. Select the Self Calibration tab page and select the logic analyzer module. Click on the Run button to start the self calibration. Upon completing the self calibration the logic analyzer module menu selection changes from Running to Calibrated.

Self Calibration for Merged Modules If you intend to merge modules, perform the self calibration on each individual module first, then perform a self calibration on the merged module set.

You can run the self calibration at any time during normal operation. To maintain measurement accuracy, perform the self calibration if more than one year has elapsed since the last self calibration.

You can check the status of the self calibration in the Calibration and Diagnostics property sheet.

If the logic analyzer module loses power during the self calibration, rerun the self calibration following the next power-on. The self calibration data generated before power was interrupted must be replaced with a complete set of new data. For best results, always perform the self calibration after at least a 30 minute warm-up.

The logic analyzer module may require several minutes to run the self calibration depending on the number of channels. Select the Calibration and Diagnostics property sheet from the System menu. Select the Self Calibration tab page and select the logic analyzer module. Click the Run button to start the self calibration. Upon completing the self calibration, the logic analyzer module menu selection changes from Running to Calibrated.

Menu Overview The logic analyzer is controlled by interactive windows through the TLA application. The TLA application consists of the following windows:

- System Window. This window provides an overview of the entire logic analyzer. Use this window to navigate through the logic analyzer.

  The center of the System window displays icons that represent hardware modules installed in the logic analyzer. The icons are linked to the other windows in the logic analyzer.

- Setup Window. A setup window exists for each module in the logic analyzer. It contains all of the setup information for the logic analyzer module such as clocking, memory depth, threshold information, and channel information. Menus and dialogs contain information to set up the window as needed.

  For the DSO, the Setup window contains setup information for each DSO channel such as the input voltage ranges, bandwidth, coupling, and termination. It also contains horizontal setup information and a link to the DSO Trigger window.

- Trigger Window. The Trigger window provides access to the logic analyzer module or DSO module trigger setups. For either module, you can specify various trigger events and trigger actions to help you capture the data that you are interested in.

- Listing Data Window. The Listing Data window displays acquired data as tabular text. Each column of data represents one group of data or other logical data information, such as time stamps. Each row of data represents a different time that the data was acquired; newer samples of data display below older samples.

- Waveform Data Window. The Waveform Data window displays acquired data as graphical waveforms. All defined channel groups display as busforms for the logic analyzer and as individual analog channels for the DSO module.

- On/Off Buttons. These buttons enable or disable the operation of the modules. Click the appropriate button to enable or disable the modules.

Refer to the online help for more information on the individual menus, icons, and fields within each window. You may also want to refer to the *Tektronix Logic Analyzer Family User Manual* for additional information.

Merged Modules

A merged module set consists of a master module and one or two slave modules connected together by a merge cable connector, and by signals on the local bus of the mainframe backplane. The local bus sends the system clock of the master module to the slave modules. Refer to the *Tektronix Logic Analyzer Family User Manual* for detailed merging instructions.

Merging Rules

The following LA module merging rules must be followed:

- Only modules with 102 channels or more can be merged.
- The modules must be physically adjacent, and physically connected.
- Modules of unequal clock rate cannot be merged. All maximum sync rates must match for the entire merged set.
- Merged modules of unequal memory depths will assume the depth of the shallowest module.
- When merging two modules of unequal channel widths, use the module with the higher number of channels as the master module.
- When merging three modules of unequal channel widths, use the module with the higher number of channels as the master module and use the module with the fewest channels as slave two. Refer to *Three Way Merge* on page 2–12 for details.
- The modules should have the same firmware version.
- Two or three TLA7Nx, TLA7Px or TLA7Qx LA modules may be merged together. Two TLA7Lx and TLA7Mx LA modules may be merged together.

  TLA7Nx, TLA7Px, or TLA7Qx LA modules may not be merged with TLA7Lx and TLA7Mx LA modules. (Even if they are connected together.)
- Merging operations may not be destructive to an established merged module set. To merge a module to an established merged set, the established merged set must first be unmerged through software. Unmerged modules are the only potential candidates to add to a merged configuration.

Two Way Merge

In a two way merge, the master module is on the left and the slave module is on the right as shown in Figure 2–3.

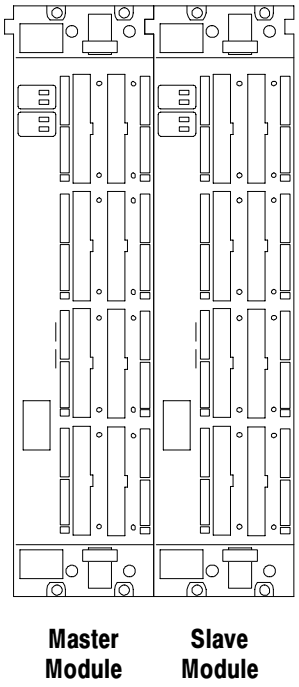


Figure 2-3: Location of modules in a two way merge

Three Way Merge

In a three way merge (TLA7Nx, TLA7Px or TLA7Qx LA modules only), the master module is in the center. Slave module 1 is to the right of the master module. Slave module 2 is on the left of the master module as shown in Figure 2–4.

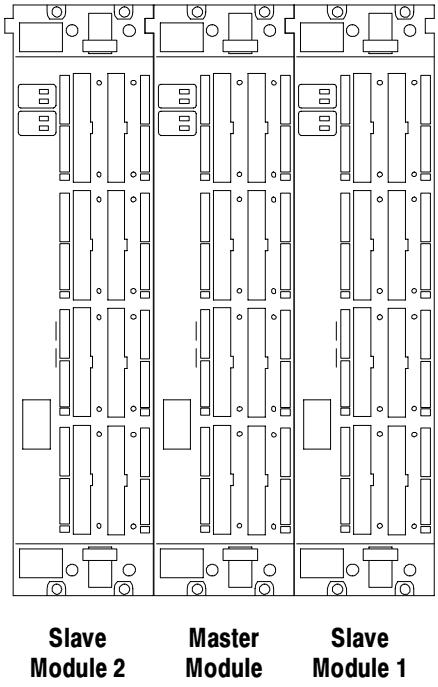


Figure 2- 4: Location of modules in a three way merge

Theory of Operation

The basic logic analyzer module consists of two main circuit boards: the LPU (local processor unit) board and the acquisition board. The logic analyzer modules with 102 or 136 channels also have one and two (respectively) comparator daughter boards present. Up to eight probes acquire data from a system under test and send it to the logic analyzer module for processing.

Block Level Description

The block level description provides an overview of each functional circuit within the logic analyzer module. Except for the number of channels, the basic operation is the same for each model.

The basic logic analyzer module consists of two main circuit boards: the Local Processing Unit (LPU) board and the Acquisition board. The logic analyzer modules with 102 or 136 channels also have one and two (respectively) Comparator Daughter boards present. Up to eight probes acquire data from a system-under-test and send it to the logic analyzer module for processing.

A single 102-channel or 136-channel logic analyzer module can be merged with a second or third module to create a two- and three-module-wide logic analyzer. Lower channel count modules do not support merging.

Local Processor Unit Board

The Local Processor Unit board controls instrument hardware, signal acquisition, power conditioning, and communications functions. Two 100-pin ribbon cables provide interconnections with the acquisition board for power supplies, data and control signals.

Processor System. The processor system contains a microprocessor that controls the entire instrument. Commands and data sent to the instrument through the mainframe pass through the communications interface, which resides on the bus. The bus also routes data between the main processor system and the acquisition board.

The processor system includes the instrument firmware. To facilitate upgrades, the firmware resides in Flash ROM.

Communications Interface. The communications interface transfers commands and data between the mainframe and the slot 0 controller. Signals pass between the instrument and the mainframe through the rear connectors.

Power Supplies. The Power Supplies receive +5 V, –5.2 V, ±12 V, and ±24 V from the mainframe through the rear connectors to power the logic analyzer module. Fuses protect the mainframe from over-current conditions. Voltage converters produce additional +5 V and +3.5 V supplies for use on the Acquisition board. The power connections to the Acquisition board are made through one of the 100-pin ribbon cables and from the backplane.

Local Processor Unit Board Fuses. Table 3–1 lists the fuses on the Local Processor Unit board and briefly describes their function.

Table 3-1: Local Processor Unit board fuses

Fuse	Voltage	Purpose
F1780	+5 V	Supplies the 5 V-to-3.5 V DC converter. The converter powers the 3 V PALS and the 3 V ASICs on the Acquisition board. The converter also enables the ±24 V-to-5 V DC to DC converter.
F1881	+5 V	Supplies the microprocessor and the supporting circuitry.
F1681	+12 V	Supplies the Control IC and MOSFET drivers for the 5 V-to-3.5 V DC to DC converter.
F1983	–24 V	Supplies the ±24 V-to-5 V DC to DC converter. This +5 V output powers the acquisition RAM on the Acquisition board.
F1981	+24 V	Supplies the ±24 V-to-5 V DC to DC converter. This +5 V output powers the acquisition RAM on the Acquisition board.

Acquisition Board

The acquisition board accepts input signals from the probes and converts them to digital information. Two 100-pin ribbon cables provide interconnections with the LPU board.

Clock Circuitry. The system clock is derived from the 10 MHz clock (from the backplane) through a phase-locked loop. The acquisition run circuitry is integrated with the clock circuitry to support time correlation.

Probe Interface. Acquisition data passes from the probe input circuitry to the probe receivers. Each probe receiver receives 16 data signals and one clock/qualifier signal.

Two threshold voltages are generated for each probe input circuit (one for the clock/qualifier signal and one for the 16 data signals). The threshold output voltages are sent to the probe receiver. The threshold adjustment procedure, performed by software, guarantees the accuracy of the reference voltages provided to the probe receivers to achieve the desired low/high logic level detection.

Acquisition System. Acquired data from the probe interface is sent to the data recognition circuitry. The data recognition circuitry analyzes the acquired data and determines which data to qualify and send to the acquisition memory. It also sends trigger event signals to the trigger and storage circuitry.

Trigger and Storage Control Circuitry. The trigger and storage control circuitry works with the data recognition circuitry. The trigger circuitry determines when to store data and when to trigger, controls counter/timers, and drives intermodule signals. The storage circuitry receives information from the trigger circuitry to determine when to start storing data and when to stop storing data.

Acquisition Memory. The acquisition memory stores acquired data. The acquisition memory can be set up to contain all data samples or it can be split to contain data samples and glitch information.

When the acquisition memory is split, half of the memory depth is lost and the logic analyzer module can only run at half speed. Each stored data sample takes up two memory locations: one to store the actual data sample, and the other to store the corresponding glitch information.

Backplane Interface. The backplane interface provides the interface with the mainframe and the Acquisition board. The interface contains intermodule signals that communicate with other modules. It also provides the 10 MHz reference clock.

Local Processing Unit Interface. The LPU interface provides the interface between the LPU circuit board and the acquisition board through two 100-pin ribbon cables (W100 and W200).

Daughter Boards

Each comparator daughter board passes 32 data signals and 2 clock/qualifier signals from the probes through two probe receiver ICs to the Acquisition board. Each prove receiver also receives two threshold voltages (four threshold signals total) from the Acquisition board. This results in 72 signal pins connecting each Daughter board to the Acquisition board.

The 136-channel logic analyzer modules have two Daughter boards; the 102-channel logic analyzer modules have only one Daughter board. No Daughter boards are present in 68-channel or 34-channel logic analyzer modules; the probe input circuitry for these modules is present on the Acquisition board.

Probes

Each P6417 probe acquires 17 channels (16 data channels and one clock or qualifier) of data.

Merged Modules

A merged module consists of a Master module and a Slave module connected together by a merge cable connector and by signals on the local bus of the mainframe backplane. The local bus sends the system clock of the Master module to the Slave module. The two merged modules must be located in adjacent slots.

The merge Cable Connector passes 26 signals between the two modules (16 trigger event signals, two storage control signals, foru valid sample clock iden tification signals, and four data-login control signals).

Performance Verification: Logic Analyzer Module

This chapter contains procedures for functional verification, certification, and performance verification procedures for the logic analyzer modules and the adjustment/verification fixture. Generally, you should perform these procedures once per year or following repairs that affect certification.

Summary Verification

Functional verification procedures verify the basic functionality of the instrument inputs, outputs, and basic instrument actions. These procedures include power-on diagnostics, extended diagnostics, and manual check procedures. These procedures can be used for incoming inspection purposes.

Certification procedures certify the accuracy of an instrument and provide a traceability path to national standards. Calibration data reports are produced for the logic analyzer modules as output from the performance verification and adjustment software. For the adjustment/verification fixture, you can make copies of the calibration data report included with this manual and then fill out the report with the data that you obtain from the performance verification procedures.

Performance verification procedures confirm that a product meets or exceeds the performance requirements for the published specifications documented in the *Specifications* chapter of this manual. Refer to Figure 4–1 on page 4–2 for a graphic overview of the procedures.

Adjustment procedures check for, and if necessary, correct any adjustment errors discovered when performing functional or performance verification procedures. The adjustment procedures for the logic analyzer modules are controlled by software while the procedures for the adjustment/verification fixture require manual intervention. Some of the adjustment procedures for the logic analyzer modules also require manual intervention to move probes or change test equipment settings.

The performance verification and adjustment software is provided on the product CD-ROM. If you have not already done so, refer to *Software Installation and Removal* beginning on page 2–2 for instructions on installing the performance verification and adjustment software.

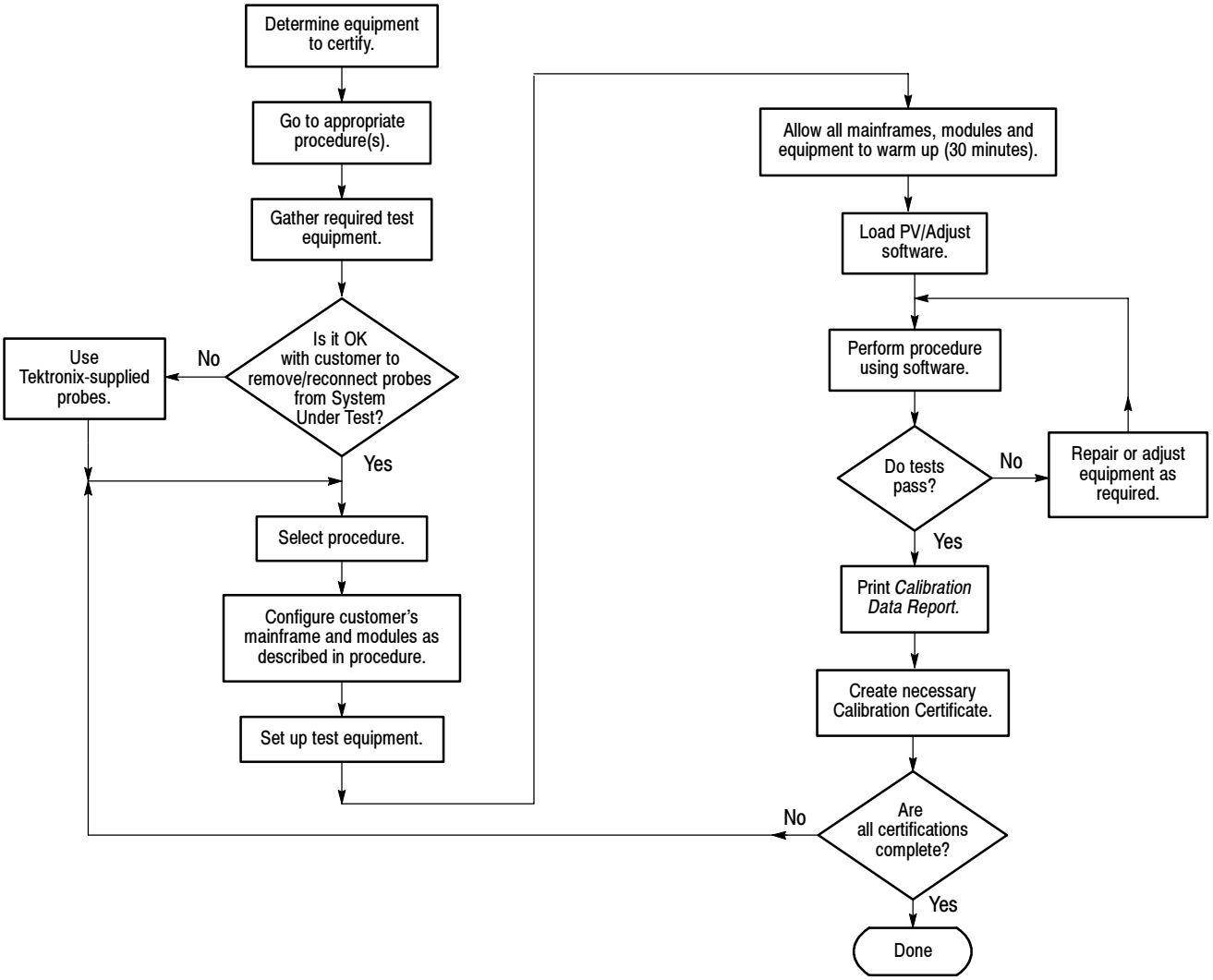


Figure 4- 1: Calibration/certification procedure flow chart

Test Equipment

The procedures use external, traceable signal sources to directly test characteristics that are designated as checked (✓) in the *Specifications* chapter of this manual. Table 4–1 shows the required equipment list; the equipment is required for the performance verification procedures and adjustment procedures for the logic analyzer modules and for the adjustment/verification fixture.

Table 4-1: Test equipment

Item number and description	Minimum requirements	Example
1. Mainframe	TLA700 Series Mainframe with a logic analyzer module installed	TLA721 Benchtop Mainframe or TLA715 Portable Mainframe
2. Adjustment/verification fixture, with one of the following		Tektronix part number 671-3599-XX
Power Supplies:		Tektronix part numbers:
USA/CAN	12 V, 1.5 A	119-4855-XX
Europe	12 V, 1.5 A	119-4856-XX
Japan	12 V, 1.5 A	119-4859-XX
United Kingdom	12 V, 1.5 A	119-4857-XX
3. Oscilloscope	1 GHz bandwidth Delay time accuracy ±25 ppm over any ≥ 1 ms interval	Tektronix TDS 784D
4. DSO probes	Two required, with < one-inch ground leads	Tektronix P6243 or P6245 probe, with accessories
5. 1X probe	One required, with < one-inch ground leads	Tektronix P6101B probe, with accessories
6. Logic analyzer probes	Two required	Tektronix P6417 or P6418 Logic Analyzer probes
7. High density logic analyzer probe (optional)	One required	Tektronix P6434 Logic Analyzer probe
8. Frequency counter	Frequency range: 1 GHz	Tektronix DC508
9. Digital multimeter with leads	DCV accuracy: 0.1% from -10 V to +100 V	Tektronix DMM 900 Series
10. Connector, dual-banana	Female BNC-to-dual banana	Tektronix part number 103-0090-XX
11. Voltage reference	Accuracy: ≤0.01%	Data Precision 8200
12. Capacitor[1]	0.1 μF, 200 V	Tektronix part number 283-0189-XX
13. Adapter, N-to-BNC	Male type N-to-female BNC	Tektronix part number 103-0045-XX
14. Shorting jumpers	Strip of 10, 2-wide	Tektronix part number 131-5829-XX
15. Cable, precision 50 Ω coaxial	50 Ω, 36 in, male-to-male BNC connectors	Tektronix part number 012-0482-XX
16. Signal Generator	250 MHz	Tektronix SG503

[1] **The capacitor is installed across the Data Precision 8200 output terminals to reduce noise. If your voltage reference produces <4 mVp-p of noise, external noise reduction is not necessary.**

Functional Verification

This section contains instructions for performing the functional verification procedures for the TLA7Nx, TLA7Px, and TLA7Qx Logic Analyzer modules; functional verification procedures for the adjustment/verification fixture begin on page 4–21. These procedures provide an easy way to check the basic functionality of the LA modules and probes.

Table 4–2 lists the functional verification procedures available for the logic analyzer modules and probes.

Table 4-2: Logic Analyzer Module functional verification procedures

Instrument	Procedure	Adjustment/verification fixture required
Single logic analyzer module	Extended diagnostics	No
Merged logic analyzer module	Extended diagnostics	No
	Merge diagnostics	No
P6417, P6418, and P6434 Logic Analyzer probe	Signal input check	Yes

If any check within this section fails, refer to the Troubleshooting section in the *Maintenance* chapter of this manual for assistance. Failed tests indicate the instrument needs to be serviced.

The functional verification procedure consists of the following parts:

- Module self tests and power-on diagnostics
- Single module procedure
- Merged module procedure
- Probe verification

This procedure provides a functional check only. If more detailed testing is required, perform the *Performance Verification Procedure* after completing this procedure.

Perform these tests whenever you need to gain confidence that the instrument is operating properly.

Test Equipment

You will need the following equipment to complete the functional verification procedure:

- TLA700 Series Logic Analyzer mainframe with one LA module installed (more modules are required to check the merged functionality)
- One adjustment/verification fixture with power supply

Setup

It is assumed that the LA module is properly installed and that all accessories are connected. Refer to the *Tektronix Logic Analyzer Family User Manual* for installation instructions.

Power on the instrument and allow a 30-minute warmup before continuing with any procedures in this section.

Module Self Tests and Power-On Diagnostics

During power-on, the installed modules perform an internal self test to verify basic functionality. No external test equipment is required. The self tests require only a few seconds per module to complete. The front-panel ARM'D and TRIG'D indicators blink during the self test. After testing completes, the front panel indicators have the following states:

- READY — Green (on)
- ACCESSED — off
- ARM'D — off
- TRIG'D — off

Next, the power-on diagnostics are run. If any self tests or power-on diagnostics fail, the instrument displays the Calibration and Diagnostics property sheet.

Single LA Module Functional Verification Procedure

The following procedure checks the basic functionality of a single LA module. Functional verification consists of running the extended diagnostics.

***NOTE**. Running the extended diagnostics invalidates any acquired data. If you want to save any of the acquired data, do so before running the extended diagnostics.*

Prerequisites	Warm-up time: 30 minutes
	Power-up diagnostics pass
	SELF_CAL passes

Perform the following steps to complete the functional verification procedures. Before beginning this procedure, be sure that no active signals are applied to the instrument. Certain diagnostic tests will fail if signals are applied to the probe during the test.

1. In the logic analyzer application, go to the System menu and select Calibration and Diagnostics.
2. Click the Extended Diagnostics tab.
3. Select the top level test and click the Run button.

   The diagnostics will perform each one of the tests listed in the menu under the module selection. All tests that displayed an Unknown status will change to a Pass or Fail status depending on the outcome of the tests.
4. Scroll through the test results and verify all tests pass.

***NOTE**. If Extended Diagnostics fail, run Self Cal for the LA module and then rerun Extended Diagnostics.*

Merged LA Module Functional Verification Procedure

The following procedure checks the basic operation of the merged modules.

***NOTE**. Running the extended diagnostics will invalidate any acquired data. If you want to save any of the acquired data, do so before running the extended diagnostics.*

Prerequisites	Warm-up time: 30 minutes
	Merge cable installed between all of the LA merged modules
	Power-up diagnostics pass
	SELF_CAL passes

Perform the following steps to complete the functional verification procedures. Before beginning this procedure, be sure that no active signals are applied to the instrument. Certain diagnostic tests will fail if signals are applied to the probe during the test.

1. In the logic analyzer application, go to the System menu and select Calibration and Diagnostics.
2. Click the Extended Diagnostics tab.
3. Select the top level test and click the Run button.

   The diagnostics will perform each one of the tests listed in the menu under the module selection. All tests that displayed an Unknown status will change to a Pass or Fail status depending on the outcome of the tests.
4. Scroll through the test results and verify all tests pass.

***NOTE**. If Extended Diagnostics fail, run Self Cal for the LA modules and then rerun Extended Diagnostics.*

Logic Analyzer Probe Functional Verification Procedure

The following procedure checks the basic operation of the probes by verifying that the probes recognize signal activity at the probe tips.

Equipment required	Adjustment/verification fixture version (item 2)
Prerequisites	Warm-up time: 30 minutes
	P6417, P6418 or P6434 probe connected[1]
	Test equipment connected as shown in Figure 4-2
	Diagnostics and SELF_CAL pass

1 **Do not mix probes; only one type of probe can be functionally verified at a time.**

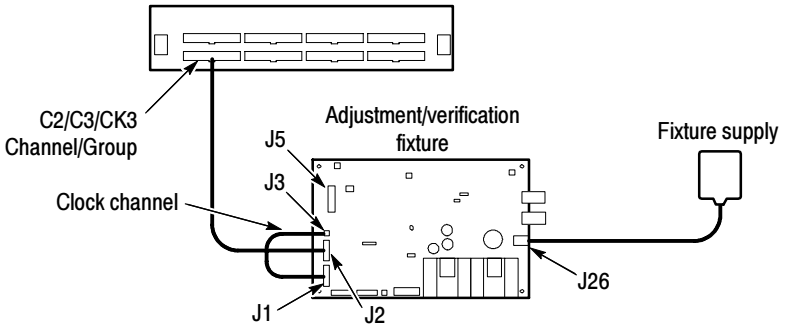


Figure 4-2: Probe functional verification test setup

Perform the following steps to complete the probe functional verification:

1. Ensure that the jumper at J15 on the adjustment/verification fixture is in the INT position to select the internal 50.065 MHz clock. See Figure 4-4 on page 4-16 for location of J15.
2. Open the Setup window for the LA module.
3. Click the Set Thresholds button to display the Probe Threshold dialog box.
4. Adjust the threshold level to 700 mV for all channels.
5. Connect the acquisition probe to be tested to the C3/C2 channel group on the LA module.
6. Refer to Figure 4-2 and connect the probe to J1 and J2 on the adjustment/verification fixture. Ensure that you connect the ground side of the podlets to the ground side of the adjustment/verification fixture connectors.

***NOTE**. These procedures assume the P6418 or P6417 probes are being used. If you have a P6434 probe, use J5, the Data Out connector on the adjustment/verification fixture for verifying probe functionality. Observe proper polarity: pin 1 to pin 1.*

7. Connect the single clock (CK n) or the qualifier (Q n) channel to one of the J3 CLK OUT connector pairs on the adjustment/verification fixture.
8. Return to the Setup window and click the Show Activity button to display the Activity Monitor.
9. Verify that the Activity Monitor shows activity on all probe channels connected to the test fixture.

   Figure 4–3 shows an example of the Activity Monitor. Note the signal activity for clock CK3 and data channels for the C3(7-0) and C2(7-0) groups. Also note that there is no activity on the other groups because the probe podlets are not connected to a signal source (the channels are all high).

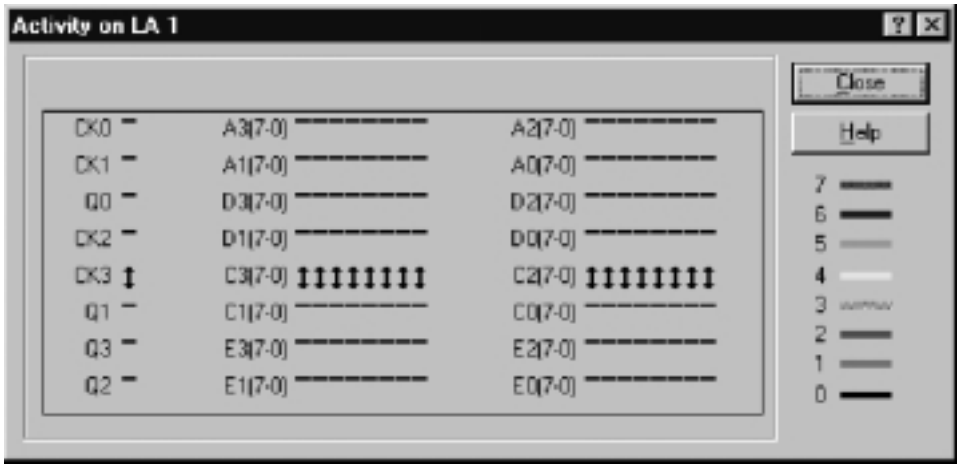


Figure 4-3: Activity Monitor

10. Verify that none of the connected channels are stuck high or stuck low.
11. Disconnect the probe from the adjustment/verification fixture and module.
12. Repeat steps 5 through 11 for any remaining probes.
13. Close the Activity Monitor.
14. Return the threshold levels to their former values in the Probe Threshold window.

LA Module Certification

Using the performance verification procedures, perform the DC Threshold test and print the software-generated Calibration Data Report. Other module specifications can also be verified by running the performance verification procedures.

Performance Verification Instructions

This section contains information to verify the performance of the LA module. Testing is performed using the performance verification and adjustment software.

The performance verification and adjustment software contains instructions and control programs for testing each characteristic designated as checked (✓) in the *Specifications* chapter of this manual.

As a general rule, these tests should be done once a year.

Prerequisites

These procedures ask for the serial number of the LA module under test. Before installing the LA module in the mainframe, record the serial number and state speed of the LA module.

Alternatively, you can access the module serial number and state speed through the logic analyzer application. In the application, go to the System menu, select System Properties, and then click the LA module tab. However, you must quit the logic analyzer application before continuing with the performance verification procedures.

The tests in this section comprise an extensive, valid confirmation of performance and functionality when the following requirements are met:

- When multiple LA modules of the same model number are installed in the mainframe, the performance verification and adjustment software will address only the module in the highest-numbered slot.

  If you are testing a TLA7Q4 module for example, move it to a higher slot number than all other TLA7Q4 modules in the mainframe. This method avoids unnecessary module warm-up time.

- When verifying the performance of merged modules using the same type of individual modules, the individual modules must be physically separated before continuing; refer to the *Tektronix Logic Analyzer Family User Manual* for information on merging and unmerging modules.

- The logic analyzer application must not be running.

- The performance verification and adjustment software must be loaded. Refer to *Software Installation and Removal* on page 2–2.

- The LA module must be installed in a mainframe, operating for at least 30 minutes, and operating at an ambient temperature between +20° C and +30° C.
- The LA module must have been last adjusted at an ambient temperature between +20° C and +30° C.
- The logic analyzer must be in an operating environment within the limits described in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual*.
- When verifying the performance of merged modules consisting of different types of individual modules, the merged module can be tested without separation. The performance verification and adjustment software runs independent of the logic analyzer application and does not recognize configuration settings. It is unnecessary to unmerge modules through the logic analyzer application before performing these procedures.

Procedure Overview

When using the performance verification and adjustment software, you will connect external test equipment to the LA module in response to prompts on the screen. You will connect the test signals and then instruct the program to continue. The performance verification and adjustment software automatically selects the module settings and determines the results of each test.

The results of the tests are recorded in a temporary file and are available upon test completion for completing test records for certification. To obtain partial test information you can also run individual tests or selected groups.

***NOTE**. The SELF_CAL test must run successfully before the other tests are performed. The remaining tests can then be performed in any order.*

Before testing an instrument following repair, you must first complete the adjustment procedure.

The performance verification and adjustment software contains the tests shown in Table 4–3. Each test verifies one or more parameters. All of the tests check characteristics that are designated as checked (✓) in the *Specifications* chapter. By running a full PV sequence, you will verify the performance of the LA Module.

Table 4-3: LA Module performance verification tests

Performance verification test name	Specification tested
1. FPV_DC_THRESHOLD[1]	Threshold accuracy
2. FPV_SETUP_0F	Setup time
3 FPV_HOLD_0F	Hold time
4. FPV_MAXSYNC	Maximum synchronous clock rate

1 Certifiable parameter

Table 4–4 lists the additional characteristics that are designated as checked (✓) in the *Specifications* chapter. These characteristics are indirectly tested by the performance verification and adjustment software tests named in the table.

Table 4-4: LA Module characteristics indirectly checked by the performance verification tests

Performance verification test name	Specification tested
1. FPV_SETUP_0F	Minimum recognizable word[1,2]
2 FPV_HOLD_0F	Minimum recognizable word[1,2]
3. All tests	Trigger state sequence rate
4. All tests, and Extended Diagnostics	Internal sampling period[3]

1 When the setup and hold time tests are both performed, the setup and hold window size is indirectly verified.

2 When the setup and hold time tests are both performed, the channel-to-channel skew is indirectly verified.

3 When all of the tests are performed, including Extended Diagnostics, the internal sampling period is indirectly verified.

In addition to the basic system setup, you will need some of the equipment shown in Table 4–1 on page 4–3 to complete the performance verification procedures.

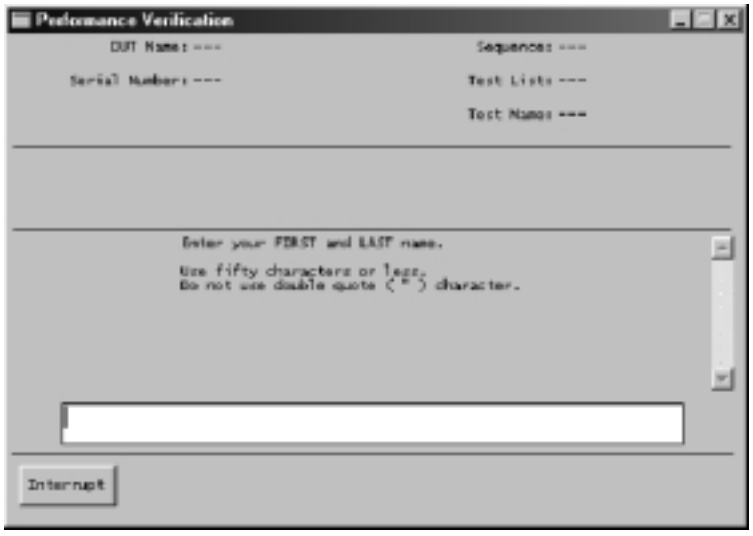
Each procedure includes a table that calls out the equipment used. Use Table 4–1 for equipment specifications. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Using the Software

The software consists of executable software files. Use the following steps to start and run the software:

1. Allow the instruments to warm up for at least 30 minutes before beginning the procedure.
2. Quit all applications including the TLA application.
3. Select Start → Programs → TLA Performance Verification.
4. To run the performance verification and adjustment software, select the following:
   - For the LA modules, select LA 7XX PV.
5. Follow the instructions on the screen to enter the name you want to appear in the User Name field as shown below. This name will appear on the Calibration Data Reports.
6. The program lists several different modules, referred to as DUT (Device Under Test). Enter the number corresponding to the module type that you want to test; then click Enter to continue.

   The screen will display an error message if the DUT chosen does not match the installed DUT.
7. Click Enter to continue.
8. Enter the complete serial number of the DUT (for example, B010100). Click Enter to continue.



If you select no, a prompt asks you to enter the serial number again.

9. The program lists sequences for PV (performance verification) and ADJ (adjustments). Enter a number to select which sequence you want and click Enter to continue.
10. If an instrument is being tested, the program lists the different probe types available for testing. Enter the appropriate number corresponding to your probe and then click Enter to continue.
11. Enter the operating temperature in degrees C (entries in the range of 20 to 30 degrees are valid). Click Enter to continue.
12. Enter the operating humidity as a percentage (0% to 100% entries are valid). Click Enter to continue.
13. Determine which sequence to run:
    - RUN FULL SEQUENCE runs the entire sequence from beginning to end. This is the recommended selection.
    - RUN PARTIAL SEQUENCE runs part of the full sequence. The sequence runs from the selected starting point to the end of the sequence.
    - SELECT TEST(S) runs only the selected tests. To run a single test, enter the test number. To run multiple tests, enter a comma-separated list of numbers or a hyphen-separated list of numbers.

    Enter the number next to your choice and click Enter to continue.
14. Follow the on-screen instructions to connect and adjust test equipment.
15. When testing is completed, disconnect the test equipment.

Using the Interrupt Button

While the program is running, you can interrupt the program to rerun a test, start over, or to exit the program by clicking the Interrupt button (shown below).

The program will then provide a list of choices. Enter the number next to the choice that you want and click Enter.

***NOTE**. If you interrupt a test before it has completed, you must restart the test to obtain valid test data.*

Some tests such as Internal Cal do not allow interrupts. If you stop these tests using more aggressive methods, you may have to reboot the instrument.

Obtaining Test Results

The results of all tests can be stored in a file on the hard disk. You can view the test results, print the test results to a printer, or save the test results in another file on the hard disk. The software stores the test results in a file containing the module name and serial number (for example, TLA7Q4.B020123). The file is located under the following path: C:\Tekcats\Rpt.

***NOTE**. If you want to save the content of the Report file, you must rename or copy the Report file using the Windows file utilities such as Explorer.*

The Report file will be overwritten the next time you run the performance verification and adjustment software and print or view a new set of test data.

After completing a full or partial test sequence (or just before you exit the program) you can generate the test data and write it to a file. You have the option of printing the file, viewing the file on screen, or transferring the file to another directory or host computer.

You can print the test data directly from the program. Ensure that a printer is connected to your logic analyzer and follow the on-screen instructions to print the test results.

If a printer is not available, you can view the test results directly from the screen, or you can copy the test results to a different file or folder/host computer for future use.

Field Adjust/PV Software Housekeeping

The performance verification and adjustment software creates data log files (.dlf files) that store program data. The .dlf files are used by the performance verification and adjustment software to generate the view data and print out options. Each .dlf file is identified by the product serial number; for example, B010100.dlf. The files are stored in the Tekcats folder under each TLA7xx folder. To conserve disk space, you must occasionally delete the .dlf files.

Troubleshooting

If any tests fail, use the following steps to troubleshoot the problems:

1. Check all test equipment for improper or loose connections.
2. Check that all test equipment is powered on and has the proper warm-up time.
3. If you are using the adjustment/verification fixture, verify the LED is lighted, the jumper positions match the on-screen instructions, and the external connections are correct. (See Figure 4–4 for jumper locations.)
4. Rerun mainframe or module diagnostics and module adjustment.
5. Run the tests a second time to verify the failure.

Performance Verification Tests

Use the following tables and figures to set up and execute each procedure.

***NOTE**. The illustrations in the following procedures show P6418 or P6417 probes. If you have a P6434 probe, use J14 on the adjustment/verification fixture for the DC Threshold test; all other procedures using the P6434 probe use J5, the Data Out connector. When using either type of probe, always observe correct polarity (GND to GND, pin 1 to pin 1).*

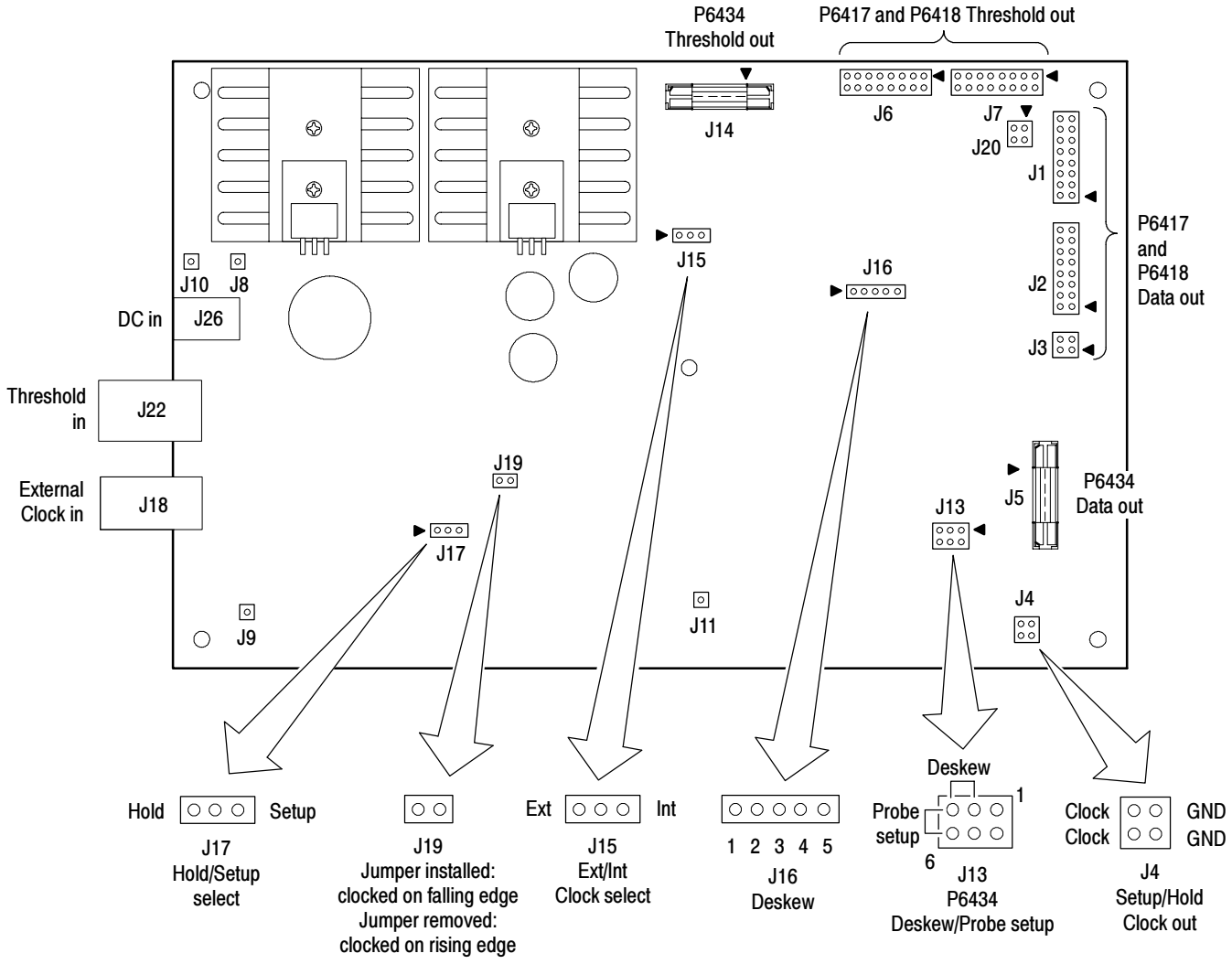


Figure 4- 4: Adjustment/verification fixture connections and jumper locations

LA Module Procedure 1: FPV_DC_Threshold

This procedure verifies the DC Threshold Accuracy of the LA Module. This test is performed once and applies to all channels of the module.

SW test name	FPV_DC_Threshold
Equipment required	Adjustment/verification fixture and fixture supply (item 2) Voltage reference (item 11) Precision BNC cable (item 15) Dual banana-to-BNC adapter (item 10) Capacitor, 0.1 μF (item 12)
Prerequisites	Warm-up time: 30 minutes Test equipment connected as shown in Figure 4-5 Diagnostics and SELF_CAL pass

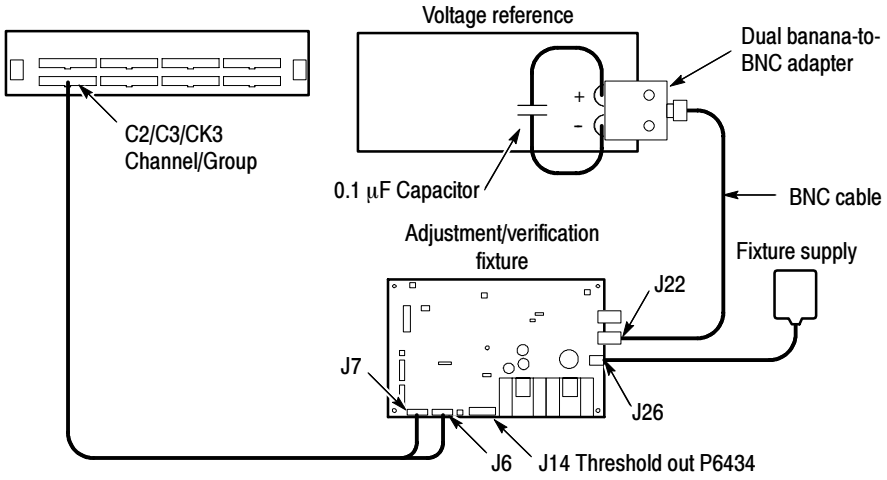


Figure 4-5: FPV_DC_Threshold test setup

1. If the logic analyzer application is running, quit the application. Verify that all of the prerequisites listed previously are met for the procedure.
2. Run the performance verification and adjustment software as described in *Using the Software* on page 4-13. Run the C:\Tekcats\Tla_la program and then select the correct module type and the PV test option.
3. Follow the on-screen instructions to run each portion of the test for each parameter of the instrument.
4. Verify that all of the tests pass.

LA Module Procedure 2: FPV_Setup_0F

This procedure verifies the setup time of the LA module.

SW test name	FPV_Setup_0F
Equipment required	Adjustment/verification fixture and fixture supply (item 2)
Prerequisites	Warm-up time: 30 minutes Test equipment connected as shown in Figure 4-6 Diagnostics and SELF_CAL pass

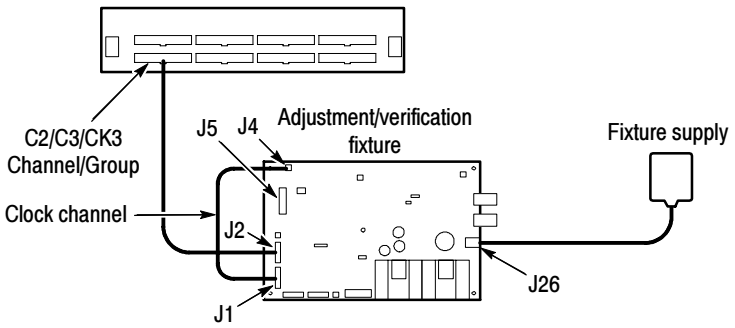


Figure 4-6: Initial FPV_Setup_0F test setup

1. If the logic analyzer application is running, quit the application and verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run each portion of the test for each parameter of the LA module.
3. Verify that all of the tests pass. If a test fails, run the Deskew routine as described on page 5-8, then rerun the test.

LA Module Procedure 3: FPV_Hold_0F

This procedure verifies the hold time of the LA Module.

SW test name	FPV_Hold_0F
Equipment required	Adjustment/verification fixture and fixture supply (item 2)
Prerequisites	Warm-up time: 30 minutes Test equipment connected as shown in Figure 4-7 Diagnostics and SELF_CAL pass

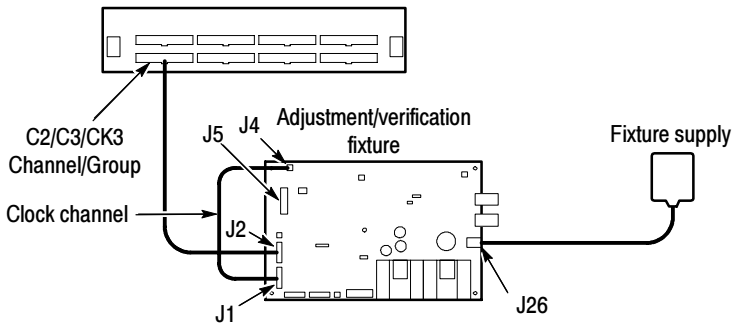


Figure 4-7: Initial FPV_Hold_0F test setup

1. If the logic analyzer application is running, quit the application and verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run each portion of the test for each parameter of the LA module.
3. Verify that all of the tests pass. If a test fails, run the Deskew routine as described on page 5-8, then rerun the test.

LA Module Procedure 4: FPV_Maxsync

This procedure checks the Maximum Synchronous Clock Rate and the Trigger State Sequence Rate of the LA Module. This test is performed once and applies to all channels of the module.

SW test name	FPV_Maxsync
Equipment required	Adjustment/verification fixture and fixture supply (item 2) Sine wave generator (item 16) BNC cable (item 15) Adapter, N-to-BNC (item 13)
Prerequisites	Warm-up time: 30 minutes Test equipment connected as shown in Figure 4-8 Diagnostics and SELF_CAL pass

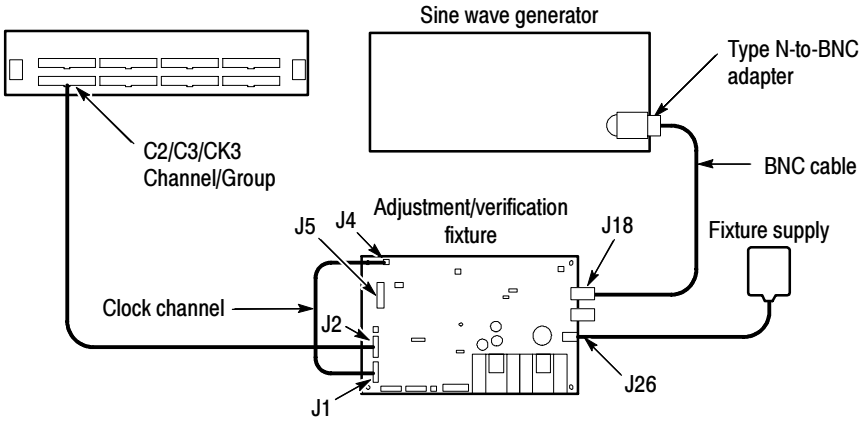


Figure 4-8: FPV_Maxsync test setup

1. If the logic analyzer application is running, quit the application and verify that all of the prerequisites listed previously are met for the procedure.
2. Follow the on-screen instructions to run the test.
3. Verify that all of the tests pass.

After completing the performance verification procedures, obtain a copy of the test results and verify that all parameters are within the allowable specifications as listed in the *Specifications* chapter of this manual.

Performance Verification: Adjustment/Verification Fixture

This section contains the functional verification procedures, performance verification procedures, and certification procedures for the adjustment/verification fixture. A calibration data report for the adjustment/verification fixture is also available at the end of this chapter where you can record the certifiable parameters.

Test Equipment

These procedures use external, traceable signal sources to directly test characteristics that are designated as checked (✓) in the *Specifications* chapter of this manual. Table 4–1 on page 4–3 shows the required equipment list for the procedures in this section. Each piece of equipment used in these procedures is referenced by an item number to the equipment listed in Table 4–1.

Functional Verification

The functional verification procedure consists of the following checks:

- Basic power supply verification
- External clock input circuit verification

This procedure provides a functional check only. If more detailed testing is required, perform the performance verification procedure, which begins on page 4–25, after completing this procedure.

Power Supply

Use the following procedure to verify that the fixture power supply is functional.

1. Plug the fixture power supply included with the adjustment/verification fixture into an appropriate socket and plug the DC connector into J26.
2. The LED adjacent to J26 should light. This indicates the input power supply is functioning properly.

External Clock Input

Use the following procedure to verify the external clock input circuit is dividing the input frequency by two and routing this clock signal to the proper output connectors. This test provides a basic functionality check of the adjustment/verification fixture.

Parameter tested	External clock input
Equipment required	Sine wave generator (item 16) Precision BNC cable (item 15) Oscilloscope (item 3) Oscilloscope probe (item 4)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set the jumper positions as called out in the table. Refer to Figure 4–9 on page 4–23 for jumper locations.

Jumper	Jumper name	Jumper setting
J13	P6434 Setup & Hold/Deskew select	Disconnected
J15	Clock selection	EXT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	Disconnected
J19	Clock polarity select	Disconnected

2. Connect the sine wave generator to J18, EXT CLK IN, on the adjustment/verification fixture.
3. Set the generator output to 210 MHz, 1 V p-p.
4. Set up the oscilloscope by pressing Setup, Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.

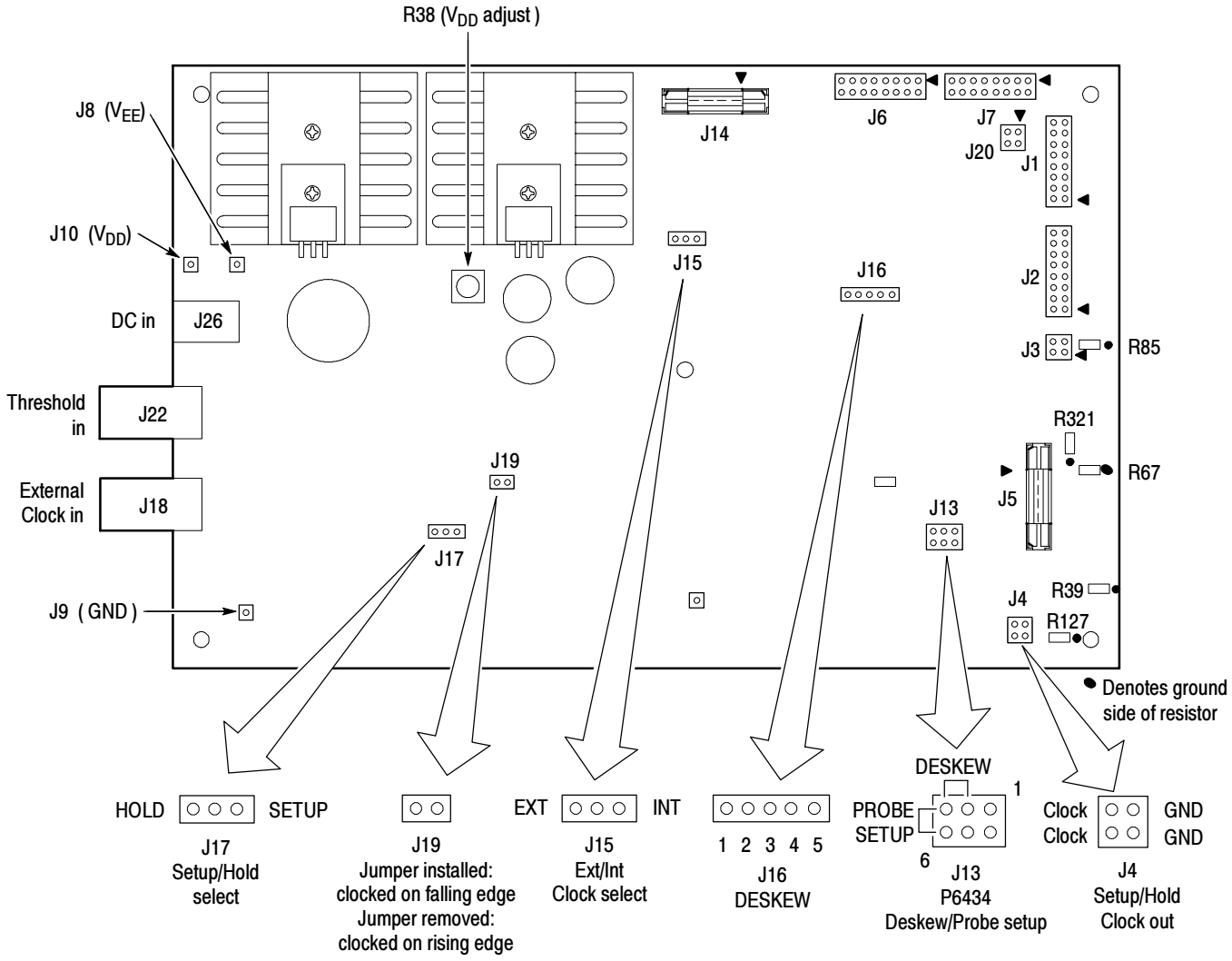


Figure 4-9: Adjustment/verification fixture detail

5. Set up the oscilloscope as listed below.

   a. Set up the CH1 Vertical menu as follows:

   - Coupling — DC/50 Ω
   - Fine Scale — 200 mV/div
   - Position — -3.32 div

b. Set up the Horizontal menu as follows:

- Time Base — Main
- Record Length — 5000
- Horizontal Scale — Main Scale @ 5 ns/div

c. Set up the Trigger menu as follows:

- Source — CH1
- Coupling — DC
- Slope — +
- Level — 700 mV
- Mode — Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 — Frequency
- Gating — Off

e. Set up the Cursor menu as follows:

- Function — Off

f. Set up the Acquire menu as follows:

- Acquisition Mode — Sample
- Repetitive Signal — On

6. Using the oscilloscope and the custom probe adapter shown in Figure 4–10 on page 4–26, verify that the output frequency at J1 pin-2 on the adjustment/verification fixture is 105 MHz.

7. Press the Run/Stop button to stop the acquisition.

8. Disconnect the test equipment from the adjustment/verification fixture.

9. This completes the functional verification procedures for the adjustment/verification fixture.

Certification

The internal system clock and clock output timing are checked for accuracy. The adjustment/verification fixture accuracy is certifiable if these parameters meet specifications.

The procedure is described in the performance verification section, beginning on page 4–25. Make a copy of the Calibration Data Report at the end of this chapter and then record the results on the copy.

Performance Verification

This section contains procedures to verify the accuracy of the adjustment/verification fixture.

Prerequisites

The tests in this section provide a valid confirmation of performance and functionality when the following requirements are met:

- The adjustment/verification fixture must have been operating for a warm-up period of at least 30 minutes, and must be operating at an ambient temperature between +20° C and +30° C.
- The adjustment/verification fixture must have been last adjusted at an ambient temperature between +20° C and +30° C.
- The adjustment/verification fixture must be in an environment within the same limits as for the logic analyzer, described in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual*.

These tests should be performed once every two years.

Tests Performed

Each test verifies one or more parameters.

Table 4-5: Adjustment/verification fixture performance verification tests

Test name	Specification tested
Power supply	V_{DD}
Internal clock frequency[1]	50.065 MHz
Data skew[1]	Less than 50 ps between any 2 channels
Hold time[1]	0.0 ns
Setup time[1]	+3.0 ns

[1] **Certifiable parameter**

Custom Probe Tip Adapter

A custom probe tip adapter is used in these procedures to ensure signal integrity when making precise measurements. The primary function of the custom probe tip adapter is to minimize the length of the ground lead of the probe. Build the custom probe tip adapter as shown in Figure 4–10.

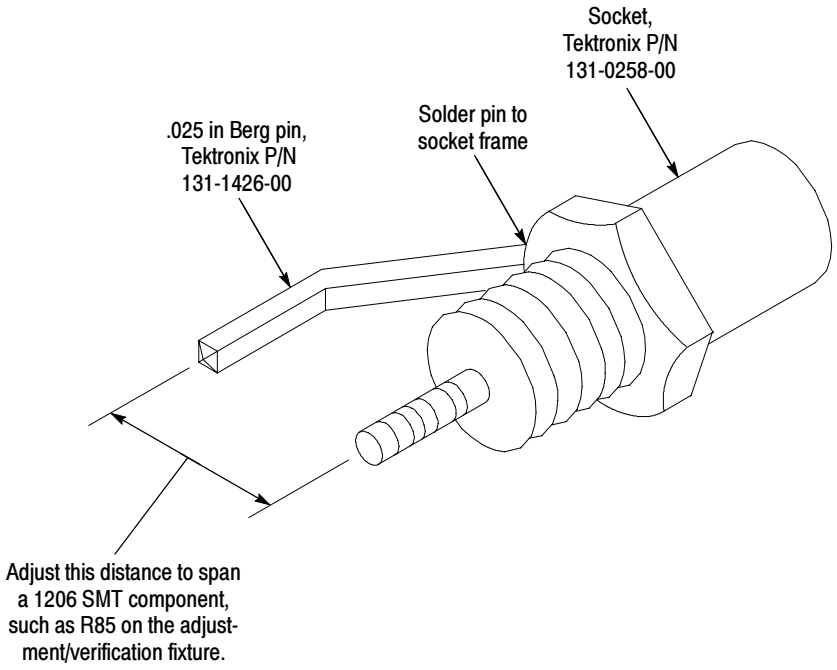


Figure 4- 10: Probe tip adapter detail

Test Procedures

Refer to Figure 4–11 on page 4–28 for component and test point locations used in the following procedures. Table 4–6 on page 4–28 describes the functions of the jumpers used on the fixture for verifying the performance of the Tektronix logic analyzers. The jumpers are also used in these procedures.

All procedures must be followed sequentially. If any single step fails or is out of calibration, then upon retest, you must start at the first test and follow this section through from start to finish sequentially.

Power Supply Checks

The following procedures check the DC power supply characteristics.

Parameter tested	Power supply
Equipment required	DMM with test leads (item 9)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Plug the fixture supply into an appropriate AC outlet and connect the DC plug to J26 on the adjustment/verification fixture.
2. Connect the DMM (–) lead to J8 (V_{EE}).
3. Connect the DMM (+) lead to J10 (V_{DD}) and verify a voltage reading of +5.00 V ±100 mV.
4. Leave the (+) lead of the DMM connected to J10 (V_{DD}) and connect the DMM (–) lead to J9 (GND). Verify a voltage reading of +2.00 V ±30 mV.

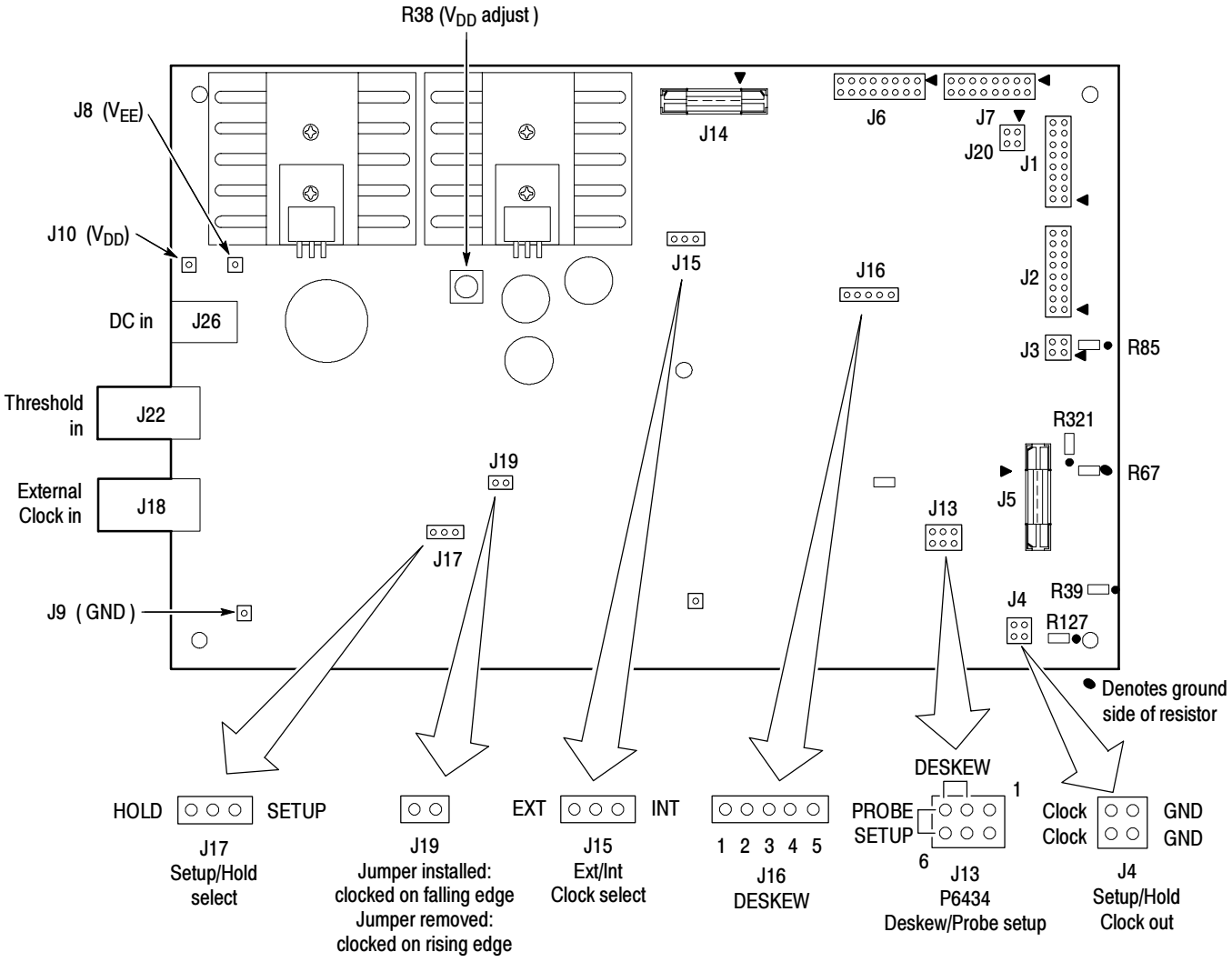


Figure 4- 11: Adjustment/verification fixture detail

Table 4- 6: Adjustment/verification fixture jumper settings

Jumper	Jumper name	Jumper function
J13	P6434 Deskew/probe setup	Determines whether checking setup/hold or deskew for the P6434 probe (J5)
J15	Clock selection	Determines whether the internal clock (50.065 MHz) or the external clock (J18, BNC) will drive the circuitry
J16	Deskew	Selects between minimum or nominal pulse width
J17	Setup/hold select	Determines whether checking setup time or hold time
J19	Clock polarity select	Selects polarity of the clock for setup and hold testing

Verify Internal Clock Frequency

Use the following procedure to verify the internal clock frequency.

Parameter tested	Internal clock frequency
Equipment required	Frequency counter (item 8)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set the jumper positions as listed in the table.

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	3-5 connected
J15	Clock selection	INT
J16	Deskew	2-3 and 4-5 connected
J17	Setup/hold select	HOLD
J19	Clock polarity select	Removed

2. Using the frequency counter, measure the oscillator frequency at pin J1-2. The frequency should match what is listed on the Calibration Data report.
3. Record this measurement on the Calibration Data Report.

Verify Data Output Channel-to-Channel Skew

Use the following procedure to verify the channel-to-channel data skew.

Parameter tested	Channel-to-channel data skew
Equipment required	Oscilloscope (item 3) 2 DSO probes (item 4) Custom probe tip adapter (see Figure 4-10, page 4-26)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set the jumper positions as listed in the following table.

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	3-5 connected
J15	Clock selection	INT
J16	Deskew	2-3 and 4-5 connected
J17	Setup/hold select	HOLD
J19	Clock polarity select	Removed

2. Set up the oscilloscope by pressing Setup, Factory Setup, and then OK Confirm Factory Init to return the oscilloscope to default conditions.
3. Set up the oscilloscope as listed below.
   a. Set up the CH1 and CH2 Vertical menu as follows:
      - Coupling DC/50 Ω
      - Fine Scale 200 mV/div
      - Position -3.00 div CH1
      - Position -3.32 div CH2

   b. Set up the Horizontal menu as follows:
      - Time Base Main
      - Record Length 5000
      - Horizontal Scale Main Scale @ 2 ns/div

c. Set up the Trigger menu as follows:

- Source CH2
- Coupling DC
- Slope +
- Level 700 mV
- Mode Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 Measure
- Gating On

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Average 90
- Repetitive Signal On

4. Connect CH2 of the oscilloscope to J4-2 on the adjustment/verification fixture.

5. Select Deskew from the Vertical menu of the oscilloscope.

***NOTE**. Observe proper polarity when doing the following steps. See Figure 4-9 on page 4-23 to identify the ground side of the components being measured.*

6. Connect the CH1 probe of the oscilloscope to the custom probe tip adapter and measure the signal across R85.

7. Use the large knob at the upper right of the oscilloscope panel to adjust delay until the leading edges of the two waveforms coincide and the displayed value of CH1-CH2 delay is averaged around 0 ±25 ps.

8. Move the CH1 probe to R321, R67, and R39 and press the Run/Stop button to start an acquisition. Verify that the CH1-CH2 delay between any two measurements does not exceed 90 ps.

9. The maximum difference between the three measured values represents the channel-to-channel skew. Record this difference on the Calibration Data Report.

Verify Hold Clock Output Timing

Use the following procedure to verify the hold time.

Parameter tested	Hold time
Equipment required	Oscilloscope (item 3) 2 DSO probes (item 4) Custom probe tip adapter (see Figure 4-10, page 4-26)
Prerequisites	Warm-up time: 30 minutes, adjustment/verification fixture and test equipment

1. Set the jumper positions as listed in the table.

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	1-3 and 5-6 connected
J15	Clock selection	INT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	HOLD
J19	Clock polarity select	Disconnected

2. Set up the oscilloscope by pressing Setup, Factory Setup, and then OK Confirm Factory Init to return the oscilloscope to default conditions.
3. Set up the oscilloscope as listed below.
   a. Set up the CH1 Vertical menu as follows:
      - Coupling DC/50 Ω
      - Fine Scale 200 mV/div
      - Position -3.00 div CH1
      - Position -3.32 div CH2
   b. Set up the Horizontal menu as follows:
      - Time Base Main
      - Record Length 5000
      - Horizontal Scale Main Scale @ 2 ns/div

c. Set up the Trigger menu as follows:

- Source CH2
- Coupling DC
- Slope +
- Level 700 mV
- Mode Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 Measure
- Gating On

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Average 90
- Repetitive Signal On

4. Connect the CH2 probe of the oscilloscope to J1-2 on the adjustment/verification fixture.

5. Select Deskew from the Vertical menu.

***NOTE**. Observe proper polarity when performing the following steps.*

See Figure 4-9 on page 4-23 to identify the ground side of the components being measured.

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6. Connect the CH1 probe of the oscilloscope to the custom probe tip adapter and measure the signal across R67.

7. Begin the acquisition by pressing the Run/Stop button.

8. Use the large knob at the upper right of the panel to adjust delay until the leading edges of the two waveforms coincide and the displayed value of CH1-CH2 delay is averaged around 0.

9. Connect the CH1 probe to R127. Verify the CH1-CH2 delay is averaged around 0 ns ±100 ps.

10. The CH1-CH2 delay represents the hold time at R127. Record the hold time at R127 on the Calibration Data Report.

11. Connect the CH1 probe to R321. Verify the CH1-CH2 delay is averaged around 0 ns ±100 ps.

12. The CH1-CH2 delay represents the hold time at R321. Record the hold time at R321 on the Calibration Data Report.

Verify Setup Clock Output Timing

Use the following procedure to verify the setup time.

Parameter tested	Setup time
Equipment required	Oscilloscope (item 3) 2 DSO probes (item 4) Custom probe tip adapter (see Figure 4-10, page 4-26)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set the jumper positions as listed in the table.

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	1-3 and 5-6 connected
J15	Clock selection	INT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	SETUP
J19	Clock polarity select	Disconnected

2. Set up the oscilloscope by pressing Setup, Factory Setup, and then OK Confirm Factory Init to return the oscilloscope to default conditions.

3. Set up the oscilloscope as listed below.

a. Set up the CH1 Vertical menu as follows:

- Coupling DC/50 Ω
- Fine Scale 200 mV/div
- Position -3.00 div CH1
- Position -3.32 div CH2

b. Set up the Horizontal menu as follows:

- Time Base — Main
- Record Length — 5000
- Horizontal Scale — Main Scale @ 2 ns/div

c. Set up the Trigger menu as follows:

- Source — CH2
- Coupling — DC
- Slope — +
- Level — 700 mV
- Mode — Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 — Measure
- Gating — On

e. Set up the Cursor menu as follows:

- Function — V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode — Average 90
- Repetitive Signal — On

4. Connect the CH2 probe of the oscilloscope to J1 pin-2 on the adjustment/ verification fixture.

5. Select Deskew from the Vertical menu of the oscilloscope.

***NOTE**. Observe proper polarity when doing the following steps. See Figure 4–9 on page 4–23 to identify the ground side of the components being measured.*

6. Connect the CH1 probe of the oscilloscope to the custom probe tip adapter and measure the signal across R67.

7. Press the Run/Stop button to stop the acquisition and read the measurement.

8. Use the large knob at the upper right of the panel to adjust delay until the leading edges of the two waveforms coincide and the displayed value of CH1-CH2 delay is averaged around 0.

9. Set one of the vertical cursors before the leading edge of the CH 2 pulse, and the other cursor after the leading edge of the CH 1 pulse.
10. Connect the CH1 probe to R127. Verify the CH1-CH2 delay is averaged around 3.0 ns ±100 ps.
11. The CH1-CH2 delay represents the setup time at R127. Record the setup time at R127 on the Calibration Data Report.
12. Connect the CH1 probe to R321. Verify the CH1-CH2 delay is averaged around 3.0 ns ±100 ps.
13. The CH1-CH2 delay represents the setup time at R321. Record the setup time at R321 on the Calibration Data Report.

Verify External Clock Input

Use the following procedure to verify the external clock input.

Parameter tested	External Clock Input
Equipment required	Frequency Counter (item 8) Signal Generator (item 16) Shorting Jumpers (item 14)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set the jumper positions as listed in the table.

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	1-3 and 5-6 connected
J15	Clock selection	EXT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	SETUP
J19	Clock polarity select	Disconnected

2. Using the signal generator, insert a 225 MHz, 1 V_{p-p} signal at J18 EXT CLK IN.
3. Using the frequency counter, verify that the data is being output at a 112.5 MHz clocked rate at J1 and J2.

Calibration Data Report

Adjustment/Verification Fixture

Instrument model number: _____

Serial number: _____ Certificate number: _____

Verification performed by: _____ Verification date: _____

Test Data

Characteristic	Specification	Tolerance	Procedure reference	Incoming data	Outgoing data
Internal clock frequency	50.065 MHz	±.01 percent (50.0600 MHz-50.0700 MHz)	Page 4-29, Step 2		
Data Output (Channel-to-Channel Skew)	50 ps	Less than 50 ps	Page 4-31, Step 8		
Setup Clock Output (at R127)	+3.0 ns	±100 ps	Page 4-36, Step 10		
Setup Clock Output (at R321)	+3.0 ns	±100 ps	Page 4-36, Step 12		
Hold Clock Output (at R127)	0.0 ns	±100 ps	Page 4-33, Step 9		
Hold Clock Output (at R321)	0.0 ns	±100 ps	Page 4-34, Step 11		

Tektronix

Logic Analyzer Module Adjustment Procedures

This chapter contains procedures which use the performance verification and adjustment software to adjust the TLA7Nx, TLA7Px, and TLA7Qx logic analyzer modules to within factory specifications. The performance verification and adjustment software contains instructions and control programs for adjusting the instrument The software describes test equipment connections and settings, selects setup parameters, and loads calibration constants into memory.

This chapter also contains adjustment procedures for the adjustment/verification fixture which begin on page 5–11.

These procedures adjust the LA Module for conformance with the warranted characteristics listed in the *Specifications* chapter of this manual.

Adjustments should be done after repair of the module or when performance verification tests have failed.

Prerequisites

These procedures ask for the serial number of the instrument under test. Before installing the modules in the mainframe, record the serial number of the LA module.

You can also access the module serial number through the logic analyzer application. In the application, go to the System menu, select System Properties, and click on the LA instrument tab. You must quit the logic analyzer application before continuing with the performance verification and adjustment software procedures.

Only trained service technicians should perform this procedure after meeting the following requirements:

- When multiple LA modules of the same model number are installed in the mainframe, the performance verification and adjustment software will address only the module in the highest-numbered slot. If you are testing a TLA7Q4 module for example, move it to a higher slot number than all of the other TLA7Q4 modules in the mainframe. This avoids unnecessary module warm-up time.
- When adjusting merged modules using the same type of individual modules, the individual modules must be physically separated.
- The logic analyzer application must not be running.

- The performance verification and adjustment software must be loaded. Refer to *Software Installation and Removal* on page 2–2.
- The LA module must be installed in a Tektronix logic analyzer mainframe.
- The instrument requires a 30-minute warm-up time in a +20° C to +30° C environment before it is adjusted. Adjustments performed before the operating temperature has stabilized may cause errors in performance.

Merged Modules

NOTE*. Only modules with channel widths of 102 or 136 channels can be merged. Up to three modules can be merged from the TLA7Nx, TLA7Px, and TLA7Qx series modules.*

When adjusting merged modules using the same type of individual modules, for example, three TLA7Q4 modules, the individual modules must be separated before continuing. See the *Tektronix Logic Analyzer Family User Manual* for instructions on separating merged modules.

NOTE*. The performance verification and adjustment software runs independent of the logic analyzer application software and does not recognize configuration settings. It is not necessary to unmerge modules through the application software before performing these procedures on merged modules.*

When adjusting merged modules using different types of individual modules, the adjustment procedure can be done on the merged module without physical separation.

NOTE*. After all of the modules have been physically merged, run the self-calibration procedure on the merged modules. To run the self-calibration procedure, go to the System menu, select Calibration and Diagnostics, and then click the Self Calibration tab.*

Using the Software

This section describes how to perform adjustments using the performance verification and adjustment software.

Performing the Adjustments

There are no manual adjustments for the LA Modules. Instead, the performance verification and adjustment software adjusts the instrument hardware using external test equipment connections that you provide in response to prompts on the screen.

Upon successful completion of each adjustment, the performance verification and adjustment software automatically loads the new calibration data into memory.

Adjustment Sequences and Dependencies

The performance verification and adjustment software allows you to run groups of adjustments, or sequences. A sequence consists of one or more individual adjustments. Normally you will perform a RUN FULL SEQUENCE, which executes each adjustment in the proper order.

The performance verification and adjustment software also provides instructions for running each adjustment individually. However, you should only perform individual adjustments while troubleshooting.

Adjustment After Repair

You must perform a full adjustment sequence following replacement of any circuit board.

Test Equipment

In addition to the basic system setup, you will need some of the equipment shown in Table 4–1 on page 4–3 to adjust the LA module.

Each procedure includes a table that calls out the equipment used. Use Table 4–1 to identify required equipment specifications. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Adjustment Instructions

This section describes how to perform adjustments using the performance verification and adjustment software.

Using the PV/Adjust Software

The performance verification and adjustment software contains instructions for performing the adjustments. The basic steps for completing the procedures follow:

1. Start the program, enter user and product identification information, temperature, and humidity.
2. If you are using P6417 or P6418 probes, label one probe as the Reference Probe, and the other probe as the Probe Under Test.
3. If you are using a P6434 probe, label the probe channel group identified as the pin 38 side as Probe A. Label the probe channel group identified as the pin 1 side as Probe B; refer to Figure 5–1.

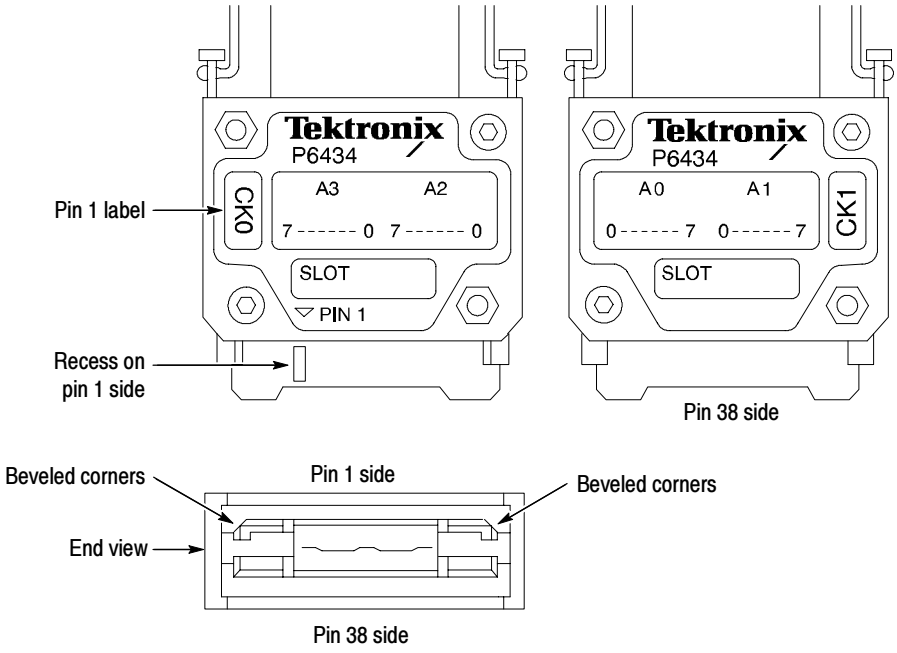

Figure 5-1: P6434 probe detail

4. Select a full adjustment sequence.
5. Connect the test equipment.

6. Set up the test equipment for the output signals described by on-screen instructions and by the connection illustration for each test.
7. Run each adjustment step as instructed by following the on-screen prompts.
8. After completing all the adjustment steps, view the results to confirm that the adjustment was successful.

When a test passes, the software automatically loads new calibration data into memory.

Troubleshooting

If any adjustments fail, use the following steps to troubleshoot the problems:

- Check all test equipment for improper or loose connections.
- Check that all test equipment is powered on and has the proper warm-up time.
- Verify the adjustment/verification fixture LED is lighted and the jumper positions match the on-screen instructions, and the external connections are correct.
- Rerun mainframe or module diagnostics and module self-cal.
- Run the adjustment procedures a second time to verify the failure.

Tests Performed

The adjustment procedures check and adjust the following parameters of the LA module:

- SELF_CAL, an internal routine in the logic analyzer application software that adjusts acquisition thresholds, internal module signal timing, and merged module signal timing.
- Deskew, an adjustment routine in the performance verification and adjustment software which time-aligns all channels.

***NOTE**. Do not mix probe types (P6417, P6418, or P6434) when performing the deskew procedure.*

Adjustment Procedures

Refer to the following procedures to identify the initial setup for each adjustment. Then follow the program instructions to complete the adjustments.

Self Calibration

Self calibration is an internal routine that optimizes performance at the current ambient temperature to maximize measurement accuracy. No external equipment or user actions are needed to complete the procedure. The LA module saves data generated by the self calibration in nonvolatile memory. Passing self cal provides a higher level of confidence of module functionality.

***NOTE**. Performing the self calibration does not guarantee that all parameters operate within limits. Operation within limits is achieved by performing the adjustment procedures. Verification of operation within limits is accomplished by performing the performance verification procedures.*

When to Perform the Self Calibration. You can run the self calibration at any time during normal operation. To maintain measurement accuracy, perform the self calibration if the following conditions occur:

- After repair and replacement of any circuit board.
- It has been a year since the last self calibration was run
- If you have just merged calibrated LA modules and received an out of calibration on-screen message. You will need to run self calibration on the merged modules.

LA Adjustment Procedure 1: SELF_CAL

Perform the following steps to run the SELF_CAL routine. Before beginning this procedure, be sure that no active signals are applied to the LA module. Self calibration can fail if signals are applied to the probe during the procedure.

Prerequisites	Warm-up time: 30 minutes Power-up diagnostics pass

1. Ensure that the instrument has had a 30-minute warm up before attempting the self calibration, and that the logic analyzer application is running.
2. Disconnect any probes connected to the LA module.
3. Select Calibration and Diagnostics from the System menu.
4. Select the Self Calibration tab page.
5. Select the LA module.
6. Click the Run button to start the self calibration.

   The self calibration takes several minutes to complete, depending on the number of channels in the module. Upon successfully completing the self calibration, the module status changes from Running to Calibrated, and the Date and Time field is set to the present.

LA Adjustment Procedure 2: Deskew

The deskew procedure calibrates and adjusts the timing alignment of the probe data channels and receivers.

Perform the deskew procedure:

- Once a year.
- If you have replaced the LPU board (the probe constants are stored on the LPU board).

This procedure checks and adjusts the time alignment of all channels. There are no manual adjustments.

SW test name	Deskew
Equipment required	Adjustment/verification fixture and fixture supply (item 2) Two P6417 or P6418 Logic Analyzer probes (item 6), OR One P6434 Logic Analyzer probe (item 7)
Prerequisites	Warm-up time: 30 minutes Test equipment connected as shown in Figure 5-2 Merged modules of the same type must be separated and deskewed separately Diagnostics and SELF_CAL pass

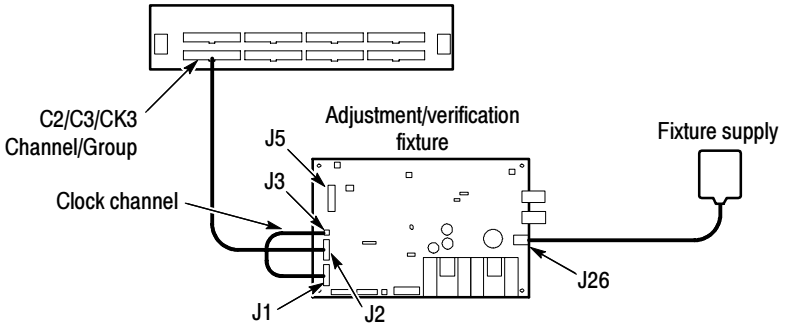

Figure 5-2: Initial deskew test setup

1. If the logic analyzer application is running, quit the application.
2. Verify that all of the prerequisites listed previously are met for the procedure.
3. Load the performance verification and adjustment software, as described in the *Software Installation and Removal* on page 2–2.

4. Run the performance verification and adjustment software. Run the C:\Tekcats\Tla_la program, then select the correct module type and the adjustment option.

***NOTE**. These procedures assume that P6418 or P6417 probes are used. If you have a P6434 probe, use J5, the Data Out connector on the adjustment/verification fixture for performing the deskew test.*

Observe proper polarity: pin 1 to pin 1.

---

5. Follow the on-screen prompts to perform the module deskew adjustment procedure.

6. Verify no failures occur for each test.

If desired, you can print or save the results of the deskew adjustment operation. However, this is not required for calibration. The file will be over-written when the next adjustment or performance verification sequence is run.

Completing the Adjustment Steps

After completing the adjustments, obtain a copy of the test results and verify that all tests passed. Run the *Performance Verification Procedures* to verify that the all parameters are within the allowable specifications as listed in the *Tektronix Logic Analyzer Family User Manual*.

Adjustment/Verification Fixture Adjustments

This section contains the adjustment procedures for the adjustment/verification fixture. Most of the adjustments consist of moving jumpers or wires that change the delays at specific locations on the board. Once these jumpers have been set (soldered) you should rarely have to change them.

Each procedure includes a table that calls out the equipment used. Use Table 4–1 on page 4–3 to identify required equipment specifications. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

Adjustment/Verification Fixture Adjustment

Equipment Required	Adjustment/verification fixture and power supply (item 2) Oscilloscope (item 3) Two 1 MΩ 10X oscilloscope probe (item 4) Frequency counter (item 8) Signal generator (item 16) 1X Probe (item 5) DMM with test leads (item 9) Shorting jumpers (item 14)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Warm up the adjustment/verification fixture and all test equipment.
   a. Connect the external power supply to fixture and perform the power supply checks and other functional steps while allowing the fixture to warm up for 20 minutes.
   b. Turn on the oscilloscope, signal generator, and frequency counter. Allow them to warm up for 20 minutes.

Power Supply Checks

The following procedure checks the DC power supply. Refer to Figure 5-3 for test point locations.

Parameter tested	Power supply
Equipment Required	DMM with test leads (item 9)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

2. Connect the DMM (-) lead to J8 (V_{EE}).
3. Connect the DMM (+) lead to J10 (V_{DD}) and check for a voltage reading of +5 V ± 0.10 V.
4. Connect the DMM negative (-) lead to J9 (GND).
5. Connect the DMM positive (+) lead to J10 (V_{DD}) and adjust R38 for a voltage reading of +2.00 V ±10 mV.

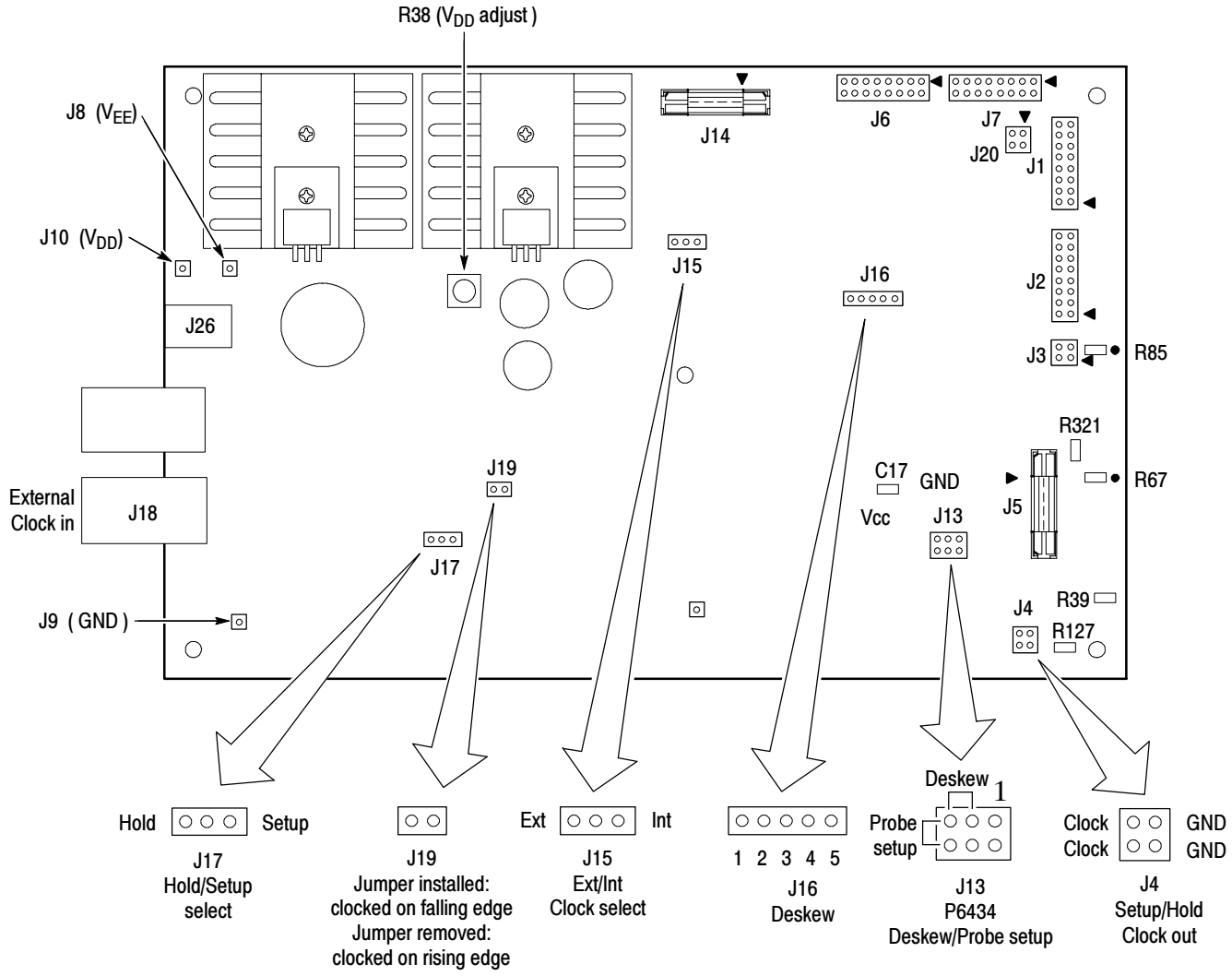

Figure 5-3: Adjustment/verification fixture circuit board layout

Internal Clock Frequency Check

The following procedure checks the internal clock frequency.

Parameter tested	Internal Clock Frequency
Equipment Required	Adjustment/verification fixture and power supply (item 2) Frequency counter (item 8) Signal generator (item 16) Shorting jumpers (item 14)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set up the frequency counter as follows:
   - **a.** Right input (10 Hz – 100 MHz)
   - **b.** Select Direct Resolution: 10 Hz
   - **c.** 1 M input termination
   - **d.** X1 Attenuation
2. Move one jumper on J16 to DESKEW (pins 2 and 3). Keep the other jumper connected to pins 4 and 5.
3. Using the frequency counter, measure the oscillator frequency at J1. It will measure 50.0650 MHz ±0.01% (50.0600 – 50.0700).

Data Pulse Width Adjustment

The following procedure adjusts the data pulse width.

Parameter tested	Data Pulse Width
Equipment Required	Adjustment/verification fixture and power supply (item 2) Oscilloscope (item 3) Two 1 MΩ 10X oscilloscope probe (item 4) Shorting jumpers (item 14)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Set up the oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.
2. Set up the oscilloscope as listed below.
   a. Set up the CH1 Vertical menu as follows:
      - Coupling DC/50 Ω
      - Fine Scale 200 mV/div
      - Position -3.32 div
   b. Set up the Horizontal menu as follows:
      - Time Base Main
      - Record Length 5000
      - Horizontal Scale Main Scale @ 1 ns/div
   c. Set up the Trigger menu as follows:
      - Source CH1
      - Coupling DC
      - Slope +
      - Level 700 mV
      - Mode Normal
   d. Set up the Measure menu as follows:
      - Select Measurement for CH1 Measure
      - Gating Off

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Sample
- Repetitive Signal On

3. Move shorting jumpers at J16 to MIN PULSE. Connect the jumpers to pins 1–2, and pins 3–4.

a. Connect the CH1 probe to J2–2. Measure the pulse width using the vertical cursor bars.

b. Using the delay taps on Delay DATA PULSE ADJ, add or subtract the appropriate delay to ensure a 1.9 ns (±50 ps) data pulse width. See Note that follows.

***NOTE**. The trace loops on the circuit board add delay according to their length. The longer the loop, the more delay is added to the circuit.*

The loops, from shortest to longest, add approximately 50 ps, 100 ps, 200 ps, 400 ps, and 800 ps respectively.

The length of the jumper wire also adds delay, so care should be used in the length of the jumper wire you add.

It will be necessary to add small loops to the wire jumpers to obtain correct delays and pulse widths on some of the following adjustments.

---

c. Move shorting jumpers at J16 to DESKEW. Connect the jumper to pins 4–5, and 2–3.

d. With the CH1 probe still connected to J2–2, measure the pulse width using the vertical cursor bars.

e. Using the delay taps on Delay DESKEW PULSE ADJ add or subtract the appropriate delay to ensure a 8–10 ns pulse width. See Note following step b.

Data Timing Adjustment

The following procedure is used to adjust the timing.

Parameter tested	Data Timing Adjustment
Equipment Required	Adjustment/verification fixture and power supply (item 2) Oscilloscope (item 3) Two 1 MΩ 10X oscilloscope probe (item 4) Shorting jumpers (item 14)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Install the following jumpers:

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	3-5 connected
J15	Clock selection	INT
J16	Deskew	2-3 and 4-5 connected
J17	Setup/hold select	HOLD
J19	Clock polarity select	Removed

1. Set up the oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.

2. Set up the oscilloscope as listed below.

a. Set up the CH1 Vertical menu as follows:

- Coupling DC/50 Ω
- Fine Scale 200 mV/div
- Position –3.32 div

b. Set up the Horizontal menu as follows:

- Time Base Main
- Record Length 5000
- Horizontal Scale Main Scale @ 200 ps/div

c. Set up the Trigger menu as follows:

- Source CH2
- Coupling DC
- Slope +
- Level 700 mV
- Mode Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 Measure
- Gating Off

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Sample
- Repetitive Signal On

3. Connect the CH2 probe to J4 and trigger on the rising edge of pulse.

4. Connect the CH1 probe to R85 (CLK0) and position the rising-edge on the center graticule.

5. Connect the CH1 probe to R67 (P6434 A) and record the positive delay between R85 and R67 using the vertical cursor bars on the oscilloscope.

6. Using the delay taps on Delay CLK1 ADJ, add or subtract the appropriate delay to ensure zero skew (±25 ps) between R85 and R67 (P6434 A). See Note on page 5–16.

7. Connect the CH1 probe to R39 (P6434 B) and record the positive delay between R85 and R39.

8. Using the delay taps on Delay CLK2 ADJ, add or subtract the appropriate delay to ensure zero skew (±25 ps) between R85 and R39 (P6434 B). See Note on page 5–16.

9. Connect the CH1 probe to R321 (P6434 deskew CLK) and record the positive delay between R85 and R321.

10. Using the delay taps on Delay DESKEW CLK ADJ (next to P6434) add or subtract the appropriate delay to ensure zero skew (±25 ps) between R85 and R321 (P6434 deskew CLK). See Note on page 5–16.

Hold Time Adjustment

The following procedure is used to adjust the hold time.

Parameter tested	Hold Time Adjustment
Equipment Required	Adjustment/verification fixture and power supply (item 2) Oscilloscope (item 3) Two 1 MΩ 10X oscilloscope probe (item 4) Shorting jumpers (item 14)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Install the following jumpers:

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	1-3 and 5-6 connected
J15	Clock selection	INT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	HOLD
J19	Clock polarity select	Removed

1. Set up the oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.

2. Set up the oscilloscope as listed below.

a. Set up the CH1 Vertical menu as follows:

- Coupling DC/50 Ω
- Fine Scale 200 mV/div
- Position -3.32 div

b. Set up the Horizontal menu as follows:

- Time Base Main
- Record Length 5000
- Horizontal Scale Main Scale @ 200 ps/div

c. Set up the Trigger menu as follows:

- Source CH2
- Coupling DC
- Slope +
- Level 700 mV
- Mode Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 Measure
- Gating Off

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Sample
- Repetitive Signal On

3. Connect the CH2 probe to J1 and trigger on the rising edge of the pulse. Connect the CH1 probe to R67 and center the rising edge on the center horizontal graticule.

4. Connect the CH1 probe to R127 and record the difference in timing between R67 and R127 using the vertical cursor bars on the oscilloscope.

5. Using the delay taps on delay labeled HOLD ADJ, add or subtract the appropriate delay to ensure zero skew (±25 ps) between R67 and R127 (J4 CLK Out). See Note on page 5–16.

6. Connect the CH1 probe to R321 and record the difference in timing between R67 and R321 using the vertical cursor bars on the (P6434 Setup/Hold timing).

7. Using the delay taps on delay labeled SU/HOLD CLK ADJ. Add or subtract the appropriate delay to ensure zero skew (±25 ps) between R67 and R321 (P6434 deskew CLK Out). See Note on page 5–16.

8. Verify that that J17 has a jumper installed in the HOLD position.

9. Connect the CH1 probe to J2 and center the rising edge on the center horizontal graticule. Trigger on the CH2 probe connected to J1.

10. Connect the CH1 probe to J4 (SU/HOLD CLK OUT) and verify for a 0 skew (±25 ps).

Setup Time Adjustment

The following procedure is used to adjust the setup time.

Parameter tested	Setup Time Adjustment
Equipment Required	Adjustment/verification fixture and power supply (item 2) Oscilloscope (item 3) Two 1 MΩ 10X oscilloscope probe (item 4) Shorting jumpers (item 14)
Prerequisites	Warm-up time: 30 minutes for adjustment/verification fixture and test equipment

1. Install the following jumpers:

Jumper	Jumper name	Jumper setting
J13	P6434 Deskew/probe setup	1-3 and 5-6 connected
J15	Clock selection	INT
J16	Deskew	1-2 and 4-5 connected
J17	Setup/hold select	SETUP
J19	Clock polarity select	Removed

1. Set up the oscilloscope by pressing Setup, and then press Factory Setup, and then press OK Confirm Factory Init to return the oscilloscope to default conditions.

2. Set up the oscilloscope as listed below.

   a. Set up the CH1 Vertical menu as follows:

   - Coupling DC/50 Ω
   - Fine Scale 200 mV/div
   - Position -3.32 div

   b. Set up the Horizontal menu as follows:

   - Time Base Main

- Record Length 5000
- Horizontal Scale Main Scale @ 500 ps/div

c. Set up the Trigger menu as follows:

- Source CH2
- Coupling DC
- Slope +
- Level 700 mV
- Mode Normal

d. Set up the Measure menu as follows:

- Select Measurement for CH1 Measure
- Gating Off

e. Set up the Cursor menu as follows:

- Function V Bars

f. Set up the Acquire menu as follows:

- Acquisition Mode Sample
- Repetitive Signal On

3. Using the delay taps on Delay SETUP ADJ., add or subtract the appropriate delay to ensure a 3.0 ns (±25 ps) timing difference between R67 and R127 (J4 – SU/HOLD CLK OUT). See Note on page 5–16.

4. Install a jumper at J19 and verify that the signal at R127 changes to a Falling Edge.

5. After completing the adjustment/verification fixture adjustment procedure, do the performance verification procedure that starts on page 4–21.

Maintenance

This chapter contains the information needed for periodic and corrective maintenance of the TLA7Nx, TLA7Px, & TLA7Qx Logic Analyzer Modules. The following sections are included.

- The *Maintenance* section provides general information on preventing damage to internal circuit boards when doing maintenance, procedures for inspecting the logic analyzer module, and cleaning external and internal circuit boards.
- The *Removal and Installation Procedures* (page 6–5) provide procedures for removing and installing circuit boards.
- *Troubleshooting* (page 6–27) provides information for isolating faulty circuit boards and probes.
- *Repackaging Instructions* (page 6–41) provides packaging information for shipment or storage.

Related Maintenance Procedures

The *TLA7UP Mainframe Field Upgrade Instruction Manual* contains some maintenance procedures not included in this manual. Refer to the *TLA7UP Mainframe Field Upgrade Instruction Manual* for information on upgrading the mainframe software or module firmware.

Preventing Electrostatic Discharge

When performing any service that requires internal access to the logic analyzer module, adhere to the following precautions to avoid damaging internal modules and their components due to electrostatic discharge (ESD).

CAUTION. *Static discharge can damage any semiconductor component*

- Minimize handling of static-sensitive modules.
- Transport and store static-sensitive modules in their static protected containers. Label any package that contains static-sensitive modules.
- Wear a grounded antistatic wrist strap while handling these modules. Service static-sensitive modules only at a static-free work station.

- Nothing capable of generating or holding a static charge should be allowed on the work surface.
- Handle circuit boards by the edges when possible.
- Do not slide the modules over any surface.

Inspection and Cleaning

Inspection and cleaning are done as preventive maintenance. Preventive maintenance, when done regularly, may prevent malfunctions and enhance reliability.

Preventive maintenance consists of visually inspecting and cleaning the logic analyzer module, and using general care when operating it. How often to perform maintenance depends on the severity of the environment in which the logic analyzer module is used. A proper time to perform preventive maintenance is just before performing adjustments on the module.

General Care

The side cover keeps dust out of the module and should be in place during normal operation.

Inspection and Cleaning Procedures

Inspect and clean the logic analyzer module as often as operating conditions require. Collection of dirt on internal components can cause them to overheat and breakdown. Dirt acts as an insulating blanket, preventing efficient heat dissipation. Dirt also provides an electrical conduction path that can cause failures, especially under high-humidity conditions.

CAUTION. *Avoid using chemical cleaning agents that might damage the plastics and external labels used in the logic analyzer module.*

Use a cloth dampened with water to clean external surfaces. To prevent damage to electrical components from moisture during external cleaning, use only enough liquid to dampen the cloth or applicator.

Use a 75% isopropyl alcohol solution to clean internal surfaces and rinse with deionized water. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

Exterior Inspection

Inspect the outside of the module for damage, wear, and missing parts. Use Table 6–1 as a guide. Instruments that appear to have been dropped or otherwise abused should be checked thoroughly to verify correct operation and performance.

Immediately repair defects that can cause personal injury or lead to further damage to the logic analyzer module or mainframe where it is used.

If you replace any electrical circuit board, refer to Table 6–8 on page 6–38 to determine which procedures you must perform to ensure proper operation of the logic analyzer module.

Table 6-1: External inspection check list

Item	Inspect for	Repair action
Front panel and side cover	Cracks, scratches, deformations, missing or damaged retainer screws, ejector handles, or EMI shields.	Replace defective or missing mechanical parts.
Front panel connectors	Broken shells, cracked insulation, and deformed contacts. Dirt in connectors.	Replace defective parts.
Rear connectors	Cracked or broken shells, damaged or missing contacts. Dirt in connectors.	Replace defective parts.
Accessories	Missing items or parts of items, bent pins, broken or frayed cables, and damaged connectors.	Replace damaged or missing items, frayed cables, and defective modules.

Exterior Cleaning Procedure

To clean the exterior, perform the following steps:

1. Remove loose dust on the outside of the logic analyzer module with a lint free cloth.
2. Remove remaining dirt with a lint-free cloth or applicator and water, using only enough liquid to dampen the cloth or applicator. Do not use abrasive cleaners.

Interior Inspection

Inspect the internal portions of the logic analyzer module for damage and wear using Table 6–2 as a guide. When found, defects should be repaired immediately.

Table 6-2: Internal inspection check list

Item	Inspect for	Repair action
Circuit boards	Loose, broken, or corroded solder connections. Burned circuit boards. Burned, broken, or cracked circuit-run plating.	Remove failed circuit board and replace with a new one.
Resistors	Burned, cracked, broken, blistered condition.	Remove failed circuit board and replace with a new one.

Table 6-2: Internal inspection check list (Cont.)

Item	Inspect for	Repair action
Solder connections	Cold solder or rosin joints.	Resolder joint and clean with isopropyl alcohol.
Capacitors	Damaged or leaking cases. Corroded solder on leads or terminals.	Remove failed circuit board and replace with a new one.
Semiconductors	Damaged parts or distorted pins.	Replace circuit board if parts are damaged.
Wiring and cables	Loose plugs or connectors. Burned, broken, or frayed wiring.	Firmly seat connectors. Repair or replace circuit boards with defective wires or cables.

CAUTION. *To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the logic analyzer module.*

Interior Cleaning Procedure

To clean the interior, perform the following steps:

1. Blow off dust with dry, low-pressure, deionized air (approximately 9 psi).
2. Remove any remaining dust with a lint free cloth dampened in isopropyl alcohol (75% solution) and rinse with warm deionized water. (A cotton-tipped applicator is useful for cleaning in narrow spaces and on circuit boards.)

NOTE*. If, after performing steps 1 and 2, a module is clean upon inspection, skip the remaining steps. If steps 1 and 2 do not remove all the dust or dirt, the module may be spray washed using a solution of 75% isopropyl alcohol (see steps 3 through 7).*

3. Gain access to the parts to be cleaned by removing easily accessible shields and panels (see *Removal and Installation Procedures* on page 6–5).
4. Spray wash dirty parts with the isopropyl alcohol and wait 60 seconds for the majority of the alcohol to evaporate.
5. Use warm (48.9° C to 60° C / 120° F to 140° F) deionized water to thoroughly rinse the parts.
6. Dry all parts with low-pressure, deionized air.
7. Dry all components and assemblies in an oven or drying compartment using low-temperature (51.7° C to 65.6° C / 125° F to 150° F) circulating air.

Removal and Installation Procedures

This section describes how to remove and install the major mechanical and electrical modules. The procedures in this section assume that you already have removed the module from the mainframe.

Preparation

Please read the following warning statement. Then read the following general instructions before removing a circuit board.

WARNING. *Before doing this or any other procedure in this manual, read the* General Safety Summary *and* Service Safety Summary *found at the beginning of this manual.*

To prevent possible injury to service personnel or damage to electrical components, read Preventing Electrostatic Discharge *on page 6–1.*

Tools Required

Most circuit boards in the TLA7Nx, TLA7Px or TLA7Qx logic analyzer module can be removed using a size T-10 Torx screwdriver. Table 6–3 lists the tools needed to replace circuit boards.

Table 6-3: Tools required for circuit board replacement

Name	Description
Screwdriver with a T-10 Torx tip	Standard tool
Soldering iron	Standard tool
Solder wick	Standard tool
1/4-inch nut driver	Standard tool

Torque Requirements

Torque all T-10 screws to 4 in. lbs.

Injector/Ejector Handles

You will need a screwdriver with a size T-10 Torx tip to replace the injector/ejector handles.

Removal

Use the following procedure and Figure 6–1 to remove the injector/ejector handles.

1. Place the module on the right side (see Figure 6–1).
2. Remove the two screws that secure the injector/ejector handle to the chassis.
3. Remove the injector/ejector handle from the module.

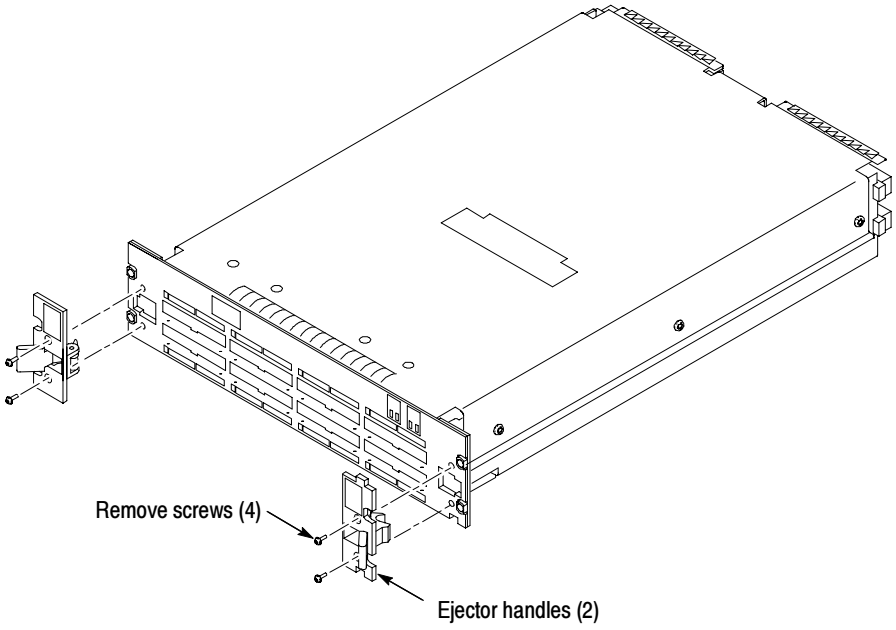

Figure 6-1: Injector/ejector handle replacement

Installation

Use the following procedure and Figure 6–1 to install the injector/ejector handles.

***NOTE**. The top and bottom injector/ejector handles are not interchangeable. The top injector/ejector handle assembly has a notch on right side and a tab on the left side; the bottom injector/ejector handle assembly does not have a notch or a tab.*

1. Install the injector/ejector handle through the front panel cutout onto the mounting post.

2. Install the screws to secure the injector/ejector handle to the chassis.
3. Apply the proper replacement label.

Cover

You will need a screwdriver with a size T-10 Torx tip to remove the cover.

Removal

Use the following procedure and Figure 6–2 to remove the cover.

1. Place the module on the right side.
2. Remove the two T-10 Torx-drive screws on the rear of the chassis and the two rear screws, located on either side of the rear panel, that secure the rear panel to the chassis.
3. Remove the four T-10 Torx-drive screws that secure the cover to the chassis.
4. If you have a 102-channel module or a 136-channel module, remove the four T-10 Torx-drive flat-head screws located near the front of the module.
5. If the merge cable is connected to the merge cable bracket, remove the two screws holding the cable and then remove the bracket.
6. Slide the cover back to disengage the tab and lift the cover from the chassis (guide the merge cable through the center hole while removing the cover).

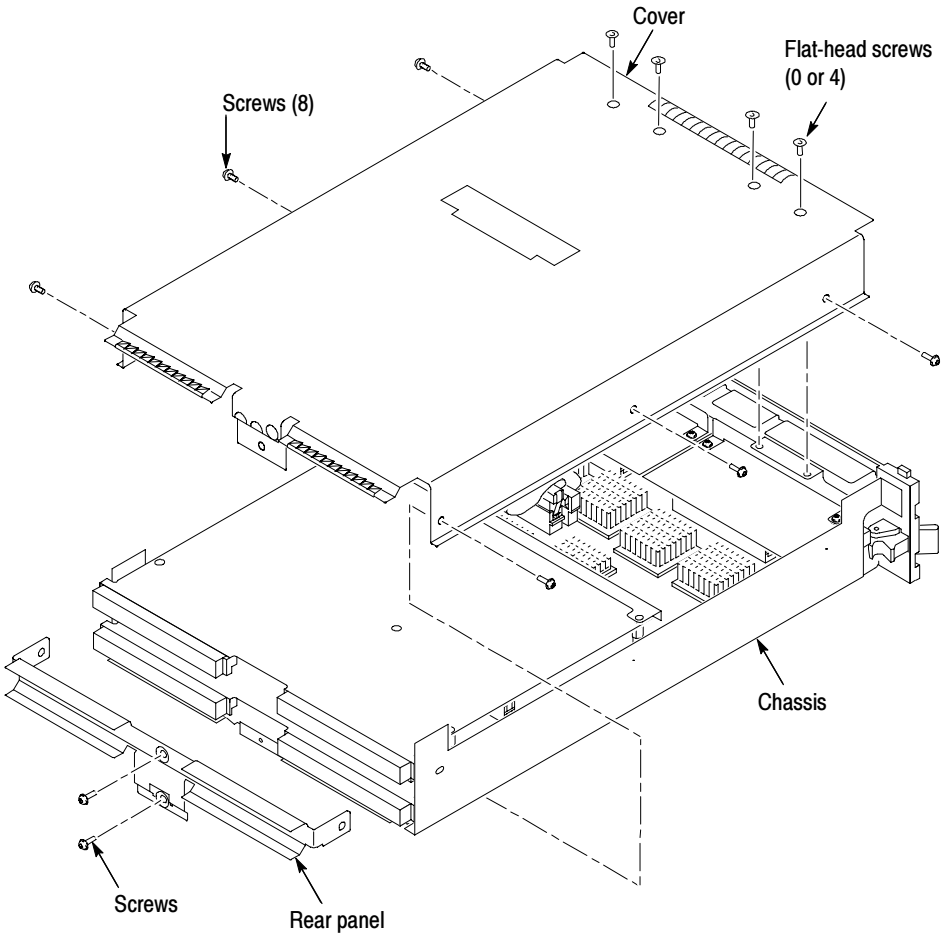

Figure 6-2: Cover removal

Installation

Use the following procedure and Figure 6–2 and Figure 6–4 to install the cover.

NOTE*. Install the cover tightly against the chassis. This will ensure that the module fits into adjacent slots in the mainframe.*

1. Place the module on its right side.
2. Place the cover onto the chassis.
3. If you are replacing the cover of the slave module in a merged module pair, refer to Figure 6–3 to feed the merge cable through the cover and then install the merge cable bracket as shown.

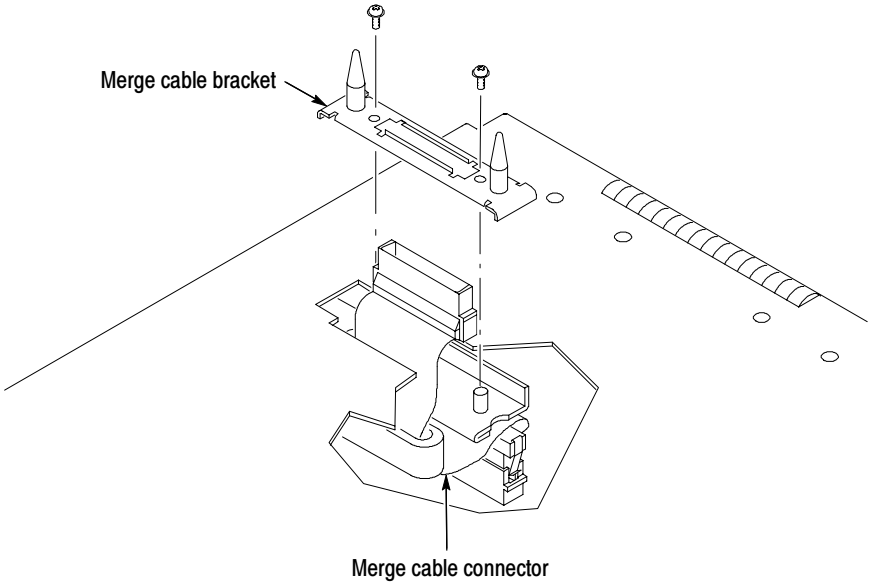

Figure 6-3: Feeding the merge cable through the cover

CAUTION. *To prevent damage to the module during the installation process, reinstall the cover exactly as described in steps 4 through 8.*

If the cover is not properly seated, the module can be damaged when you install it in a mainframe and it will not meet EMC requirements.

4. Push forward on the cover so the tab on the front edge of the cover inserts into the rear of the front subpanel. Make sure that the cover is fully seated (no gaps) against the front and rear chassis flanges (see Figure 6-4).

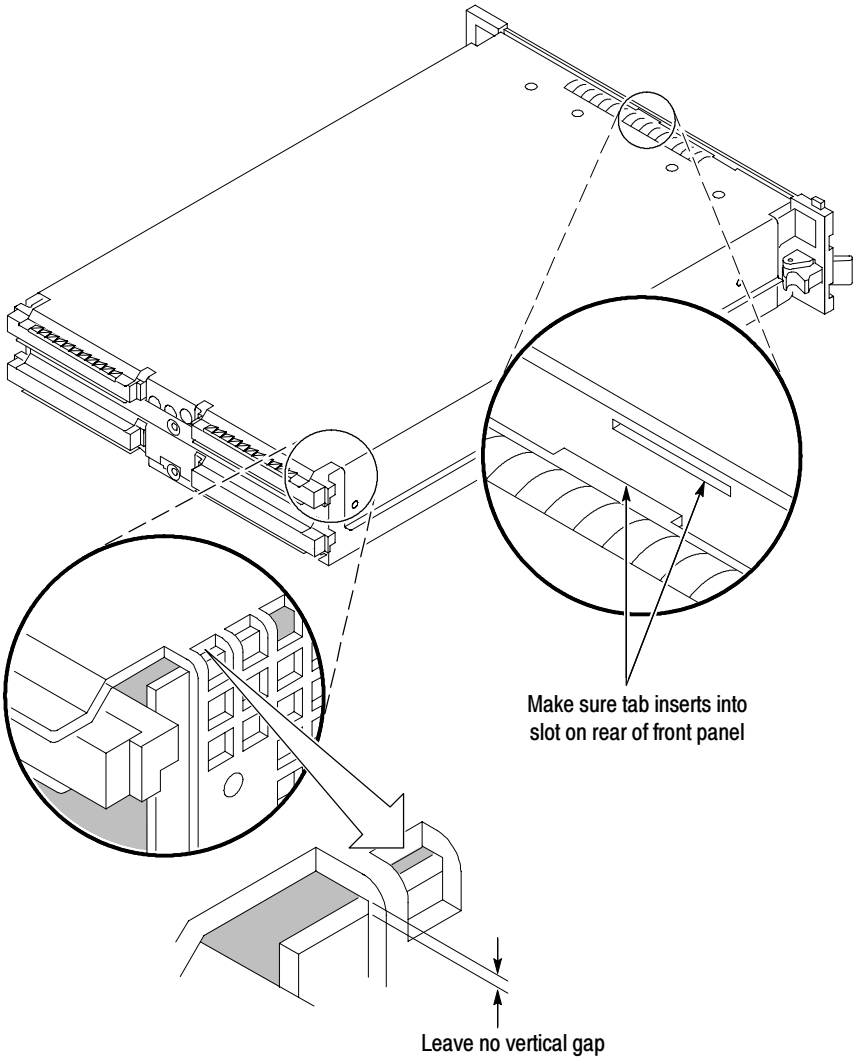

Figure 6-4: Seating the cover on the chassis

5. While holding the cover in place, install the four T-10 Torx-drive screws nearest the front of the module (two on each side of the cover), to secure the cover to the chassis.

6. If you have a 102-channel module or a 136-channel module, install the four T-10 Torx-drive flat-head screws near the front of the module.

7. Slide the rear panel on the chassis and install the two rear panel T-10 Torx-drive screws.
8. Install the two remaining T-10 Torx-drive screws nearest the rear of the module (one on each side of the cover).
9. Check and tighten all screws to 4 in lbs.

Daughter Boards

You will need a screwdriver with a size T-10 Torx tip to replace daughter boards, if applicable. It is not necessary to remove the local processor unit board to access the daughter boards.

The number of daughter boards in your module depends on the number of channels it contains:

- 136-channel modules contain two daughter boards
- 102-channel modules contain one daughter board
- 68- and 34-channel modules do not contain daughter boards

See Figure 6–5, on page 6–12, for an example of a 136-channel module that contains two daughter boards.

***NOTE**. Refer to Table 6–8 on page 6–38 and Table 6–9 on page 6–39 to determine the proper procedures to perform post-repair adjustments and to verify proper operation of the logic analyzer module.*

Removal

Use the following procedure and Figure 6–5 to remove the daughter boards.

1. Perform the *Cover* removal procedure (see page 6–7).
2. Remove the two T-10 Torx-drive screws that secure each EMI bracket and daughter board to the acquisition board.
3. Lift the daughter board straight up to disconnect it from the acquisition board connector.

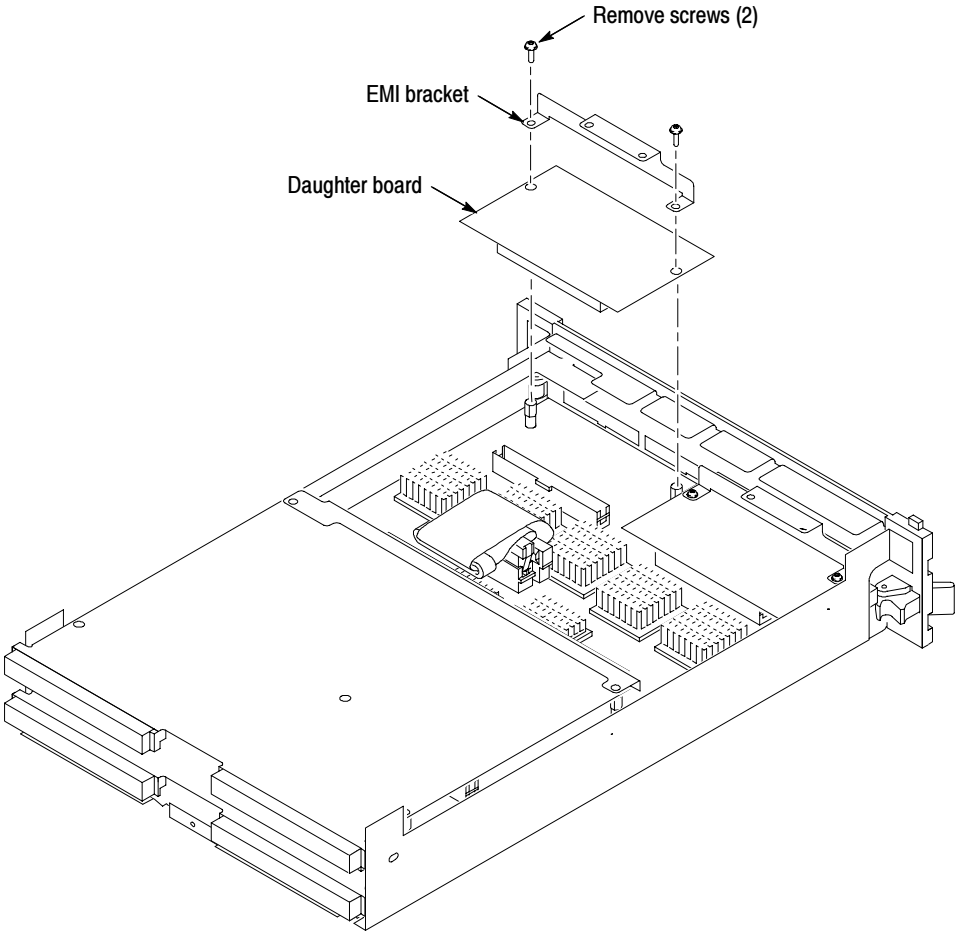

Figure 6- 5: Daughter board replacement

Installation

Use the following procedure and Figure 6–5 to install the daughter boards.

1. Line up the daughter board over the circuit board connector on the acquisition board and gently press down until the daughter board fully seats in the connector.
2. Place the EMI bracket on the daughter board.
3. Install the two T-10 Torx-drive screws that secure the EMI bracket and the daughter board to the acquisition board.
4. Perform the *Cover* installation procedure (see page 6–8).

Local Processor Unit Board

You will need a screwdriver with a size T-10 Torx tip to replace the LPU board.

***NOTE**. When placing an order for a replacement LPU board or an LPU exchange board from the Tektronix Exchange Center, you must supply the model number, serial number, PowerFlex Option upgrade number and firmware level.*

Removal

Use the following procedure and Figure 6–6 to remove the LPU board.

1. Perform the *Cover* removal procedure (see page 6–7).
2. Remove the five T-10 Torx-drive screws that secure the LPU board to the chassis.
3. Remove the cable bracket and unplug two 100-pin ribbon cables from J1330 and J1630.
4. For 102-channel modules or 136-channel modules, remove the two screws that secure the top EMI bracket to the chassis.
5. Remove the top EMI bracket to gain access to the front of the LPU board.

***CAUTION.** Handle the LPU board gently to avoid breaking the front panel LED extension.*

6. Carefully move the LPU board away from the front panel until the tabs (Figure 6–6) clear the front subpanel.
7. Lift the LPU board above the chassis.

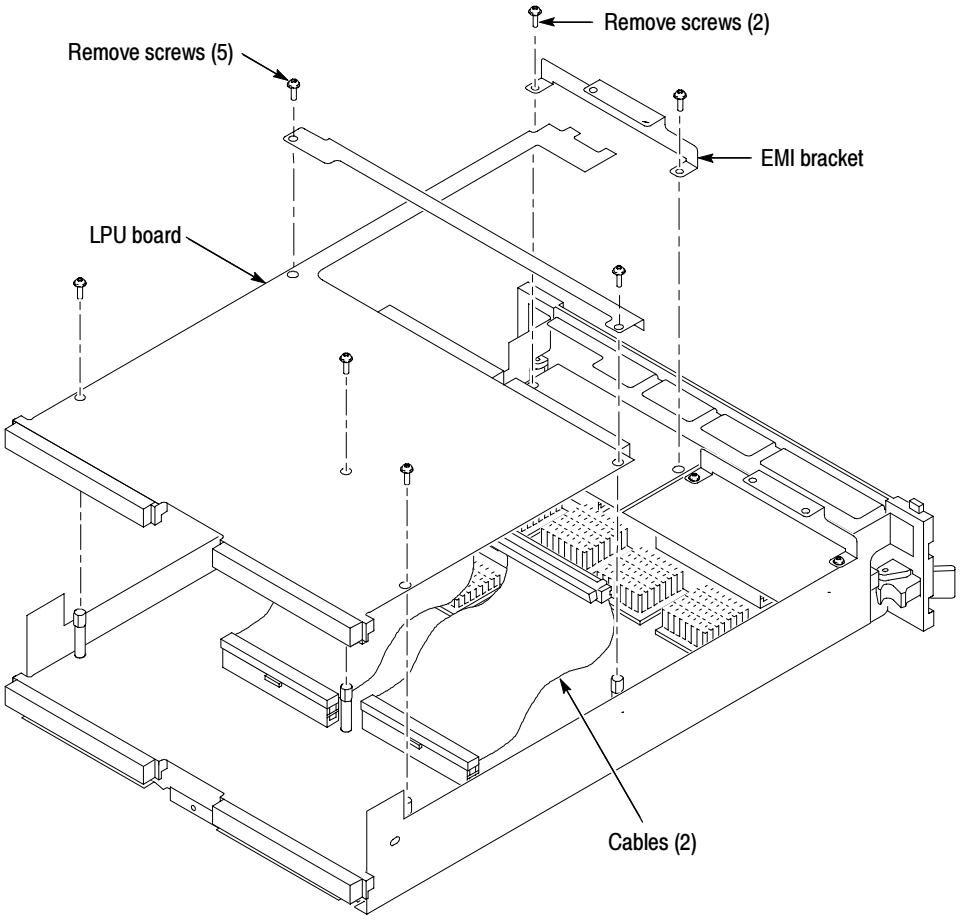

Figure 6-6: LPU board removal

Installation

Use the following procedure and Figure 6–6 to install the LPU board.

1. Insert the tabs on the LPU board into the front subpanel as shown in Figure 6–7. Then set the LPU board in place on the chassis.
2. Push forward on the LPU board rear connector while aligning the LPU board until the LPU board is even with the acquisition board.
3. Reinstall the top EMI bracket, if you removed it in step 4 on page 6–13; reinstall and tighten the two T-10 Torx-drive screws that hold the EMI bracket in place.

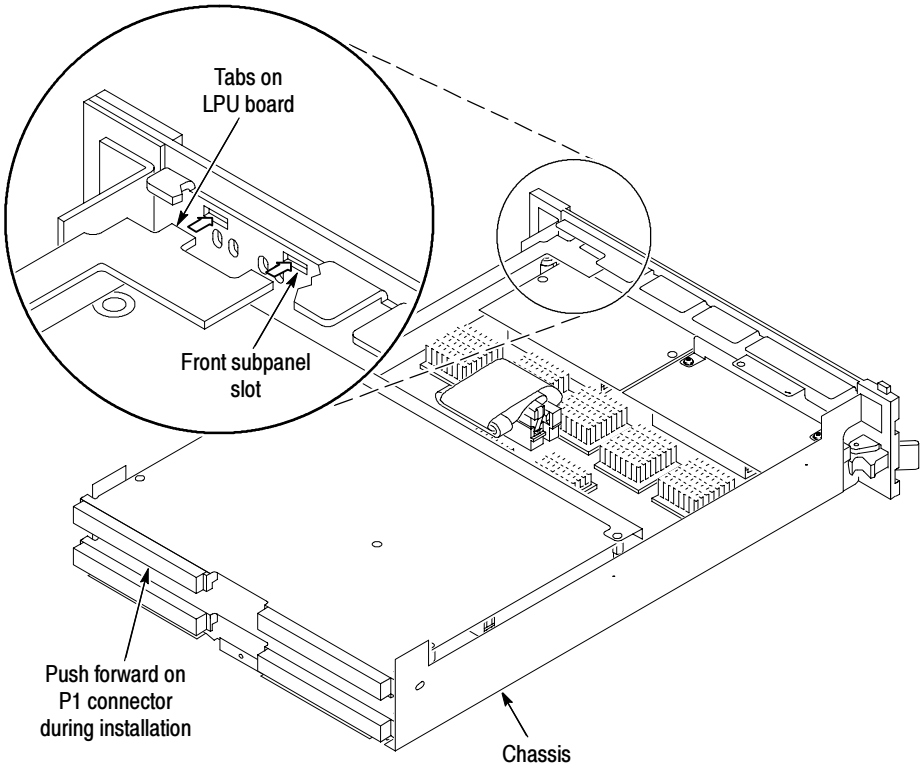

Figure 6-7: Inserting LPU board tabs into front subpanel

4. Crimp and fold the two 100-pin ribbon cables as shown in Figure 6–8 and then connect them to the LPU board at J1330 and J1630.

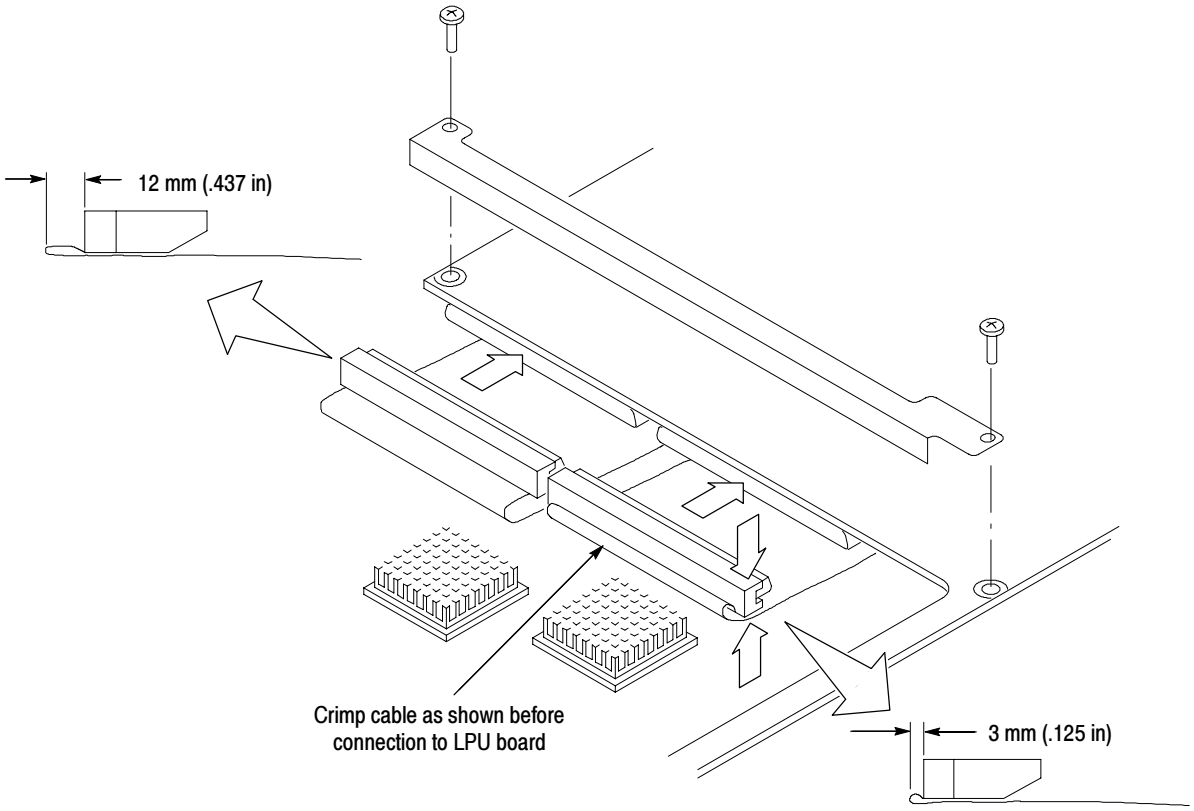

Figure 6-8: Crimping the interconnect cables

5. While holding the LPU board in place, install the cable bracket and the five T-10 Torx-drive screws that secure the board to the chassis.
6. Perform the *Cover* installation procedure (see page 6–8).

***NOTE**. After replacing the LPU board, you must verify the proper PowerFlex level. The PowerFlex configuration information is listed on the side panel of the logic analyzer module.*

If the PowerFlex level does not match the information on the side panel label, you must return the entire logic analyzer module to your local Tektronix service center.

Refer to Table 6–8 on page 6–38 and to Table 6–9 on page 6–39 to determine the proper procedures to run to verify proper operation of the logic analyzer module.

Acquisition Board

You will need a screwdriver with size T-10 Torx tip and a 1/4 inch nut driver to replace the acquisition board.

Removal

Use the following procedure and Figure 6–9 to remove the acquisition board.

1. Perform the *Cover* removal procedure (see page 6–7).
2. If there are daughter boards installed in the module, perform the *Daughter Boards* removal procedure (see page 6–11).
3. Perform the *Local Processor Unit Board* removal procedure (see page 6–13).
4. Unplug the two 100-pin ribbon cables from J1270 and J1420 as follows:
   a. Grasp and squeeze the metal cable retainers (Figure 6–9) to unlock each cable from the connector.
   b. Unplug the cables from the acquisition board and set them aside.

***NOTE**. It may be necessary to remove the spacer post between the two cables to unlock the cables from the connector.*

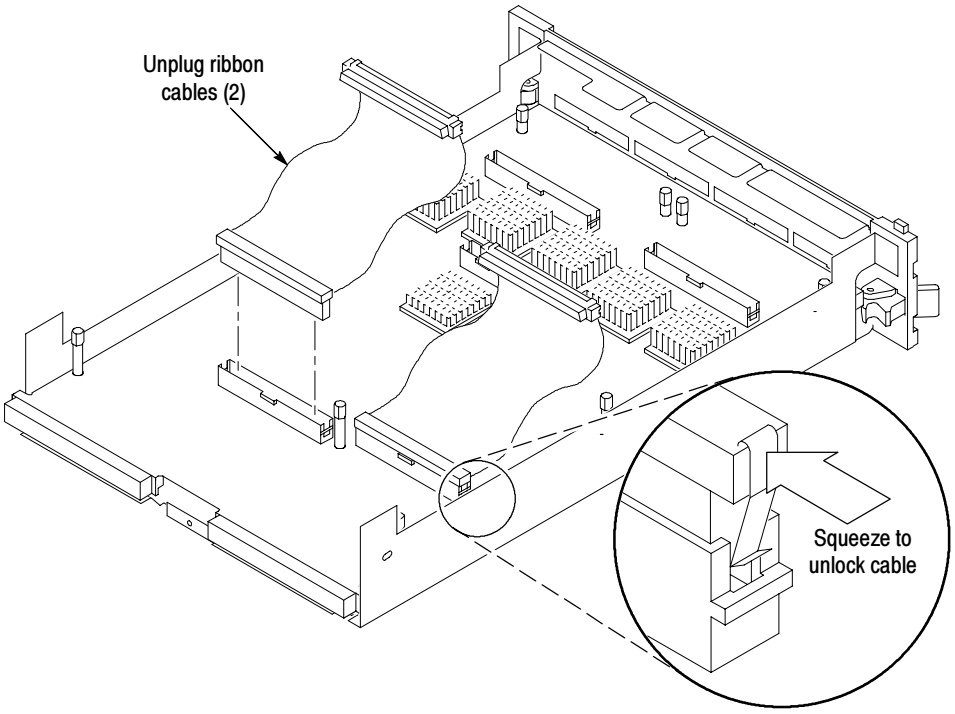

Figure 6- 9: Removing the cables from the Acquisition board

5. Turn the chassis over.

6. Remove the two screws that secure the merge cable connector to the chassis.

***NOTE**. The 34-channel and 68-channel modules do not have a merge cable or merge cable connector. For these modules, ignore the steps dealing with the merge cable and the merge cable connector.*

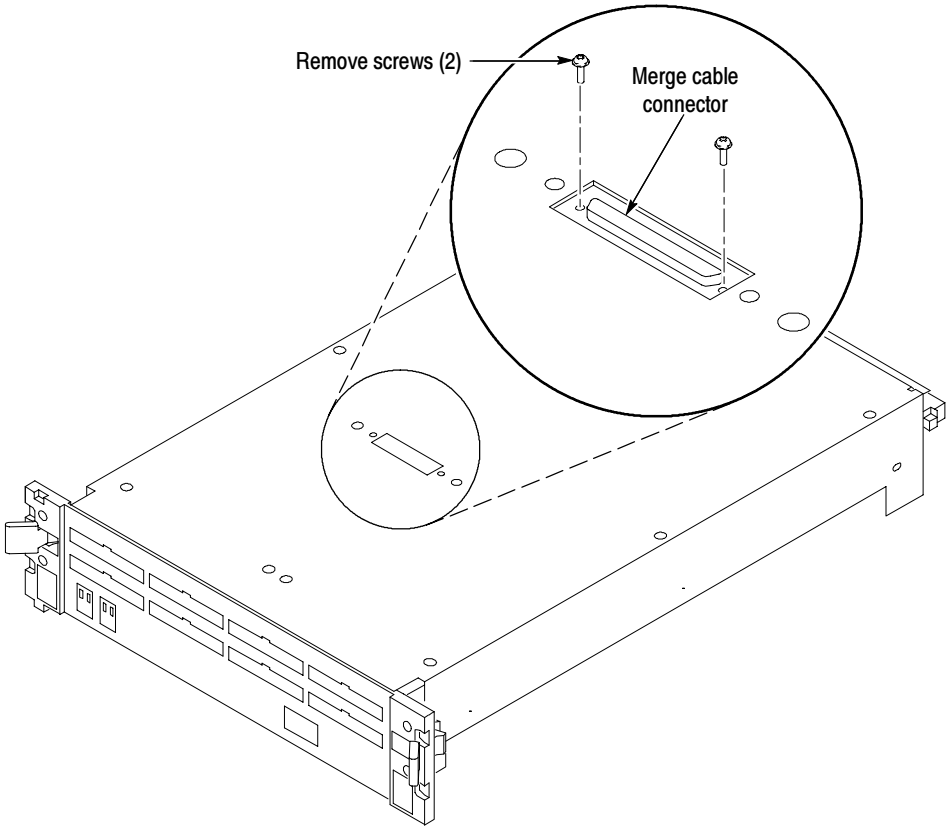

Figure 6-10: Removing the Merge cable connector from the chassis

7. Remove the nine spacer posts (with a nutdriver) that secure the acquisition board to the chassis.

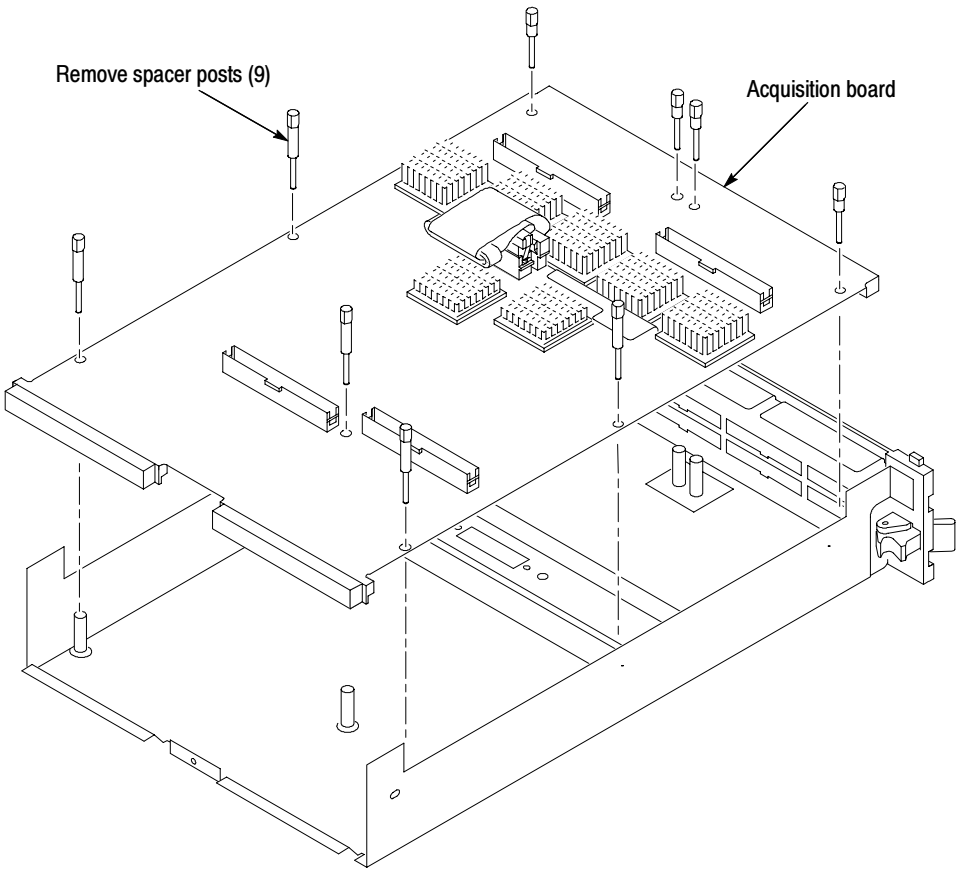

Figure 6-11: Removing the acquisition board from the chassis

8. Carefully slide the acquisition board away from the front panel until the probe connectors clear the front panel. Then lift the circuit board from the chassis.

9. Disconnect the merge cables from the acquisition board.

***NOTE**. After replacing the acquisition board refer to Table 6–8 on page 6–38 and to Table 6–9 on page 6–39 to determine the proper procedures to run to verify proper operation of the logic analyzer module.*

Installation

Use the following procedure to install the acquisition board.

1. Connect the merge cables to the acquisition board.
2. Refer to Figure 6–11 on page 6–20 and carefully slide the acquisition board into the chassis while making sure that the merge cable connector lines up with the slot in the chassis.
3. Using the screwdriver with a T-10 Torx tip, install two two screws on the merge cable connector.
4. Gently push forward on the acquisition board rear connector while aligning the acquisition board so that the mounting holes line up with the stand-offs on the chassis.
5. Install the nine spacer posts that secure the acquisition board to the chassis, ensuring that the four short spacer posts are installed near the front of the chassis.
6. Dress the top merge cable as shown in Figure 6–11 (if the module will not be merged).
7. Perform the daughter board installation procedure (see page 6–12).
8. Perform the installation procedure (see page 6–14).
9. Perform the *Cover* installation procedure (see page 6–8).

***NOTE**. After replacing the acquisition board refer to Table 6–8 on page 6–38 and to Table 6–9 on page 6–39 to determine the proper procedures to run to verify proper operation of the logic analyzer module.*

Fuses

Local Processor Unit Board Fuses

Table 6–4 lists the fuses on the LPU board and briefly describes their functions.

Table 6-4: Local Processor Unit board fuses

Fuse	Voltage	Purpose
F891	+5 V	Supplies the 5 V-to-3.5 V DC to DC converter. The converter powers the 3 V PALS and the 3 V ASICs on the acquisition board. The converter also enables the ±24 V-to-5V DC to DC converter.
F790	+5 V	Supplies the microprocessor and the supporting circuitry.
F690	+12 V	Supplies the control IC and MOSFET drivers for the 5 V-to-3.5 V DC to DC converter.
F981	-24 V	Supplies the ±24 V-to-3.3 V DC to DC converter. This +5 V output powers the acquisition RAM on the acquisition board.
F980	+24 V	Supplies the ±24 V-to-3.3 V DC to DC converter. This +5 V output powers the acquisition RAM on the acquisition board.
F890	-5 V	This supply is not used.
F470	+5 V	Supplies power to External Manufacturing FLASH card.

Acquisition Board Fuses

Table 6–5 lists the fuse locations on the acquisition board and briefly describes the fuse functions. Two columns of the following table list the acquisition board fuse circuit locations. The first column indicates where the manufacturing-installed inline fuse is located. The second column indicates the location where you can install a replacement thru-hole fuse. The parts list, located on page 10–11, contains ordering information for both types of fuses.

Table 6-5: Acquisition board fuses

Installed In-line Fuse Circuit	Replace-ment Thru-hole Fuse Circuit	Voltage	Purpose
F0952	F942	+5 V	Protect the probe receivers, DAC circuitry and local processor unit board interface.
F0950	F940	-5 V	Protect the clock circuitry.
F0941	F951	+12 V	Protect the clock circuitry and the digital to analog converter circuitry.
F0943	F953	-12 V	Protect the clock circuitry and the digital to analog converter circuitry.

Table 6-5: Acquisition board fuses (Cont.)

Installed In-line Fuse Circuit	Replace-ment Thru-hole Fuse Circuit	Voltage	Purpose
F991	F0992	-24 V	Protects the -24 V to the local processor unit board. The -24 V power a ±24 V-to-3.3 V DC to DC converter that powers the acquisition RAM.
F990	F0993	+24 V	Protects the +24 V to the local processor unit board. The voltages power ±24 V-to-3.3 V DC to DC converter that +5 V powers the acquisition RAM.

You will need a screwdriver with a size T-10 Torx tip, a soldering iron, and solder wick to replace the fuses.

Removal

Use the following procedure and Figure 6–12 to remove the fuses.

1. Perform the *Local Processor Unit Board* removal procedure (see page 6–13).
2. Use Figure 6–12 to locate the fuse to be replaced on the component side of the boards. For fuses mounted on the back side of the acquisition board, perform the Acquisition Board removal procedure (see page 6–17).
3. Unsolder and discard the fuse.

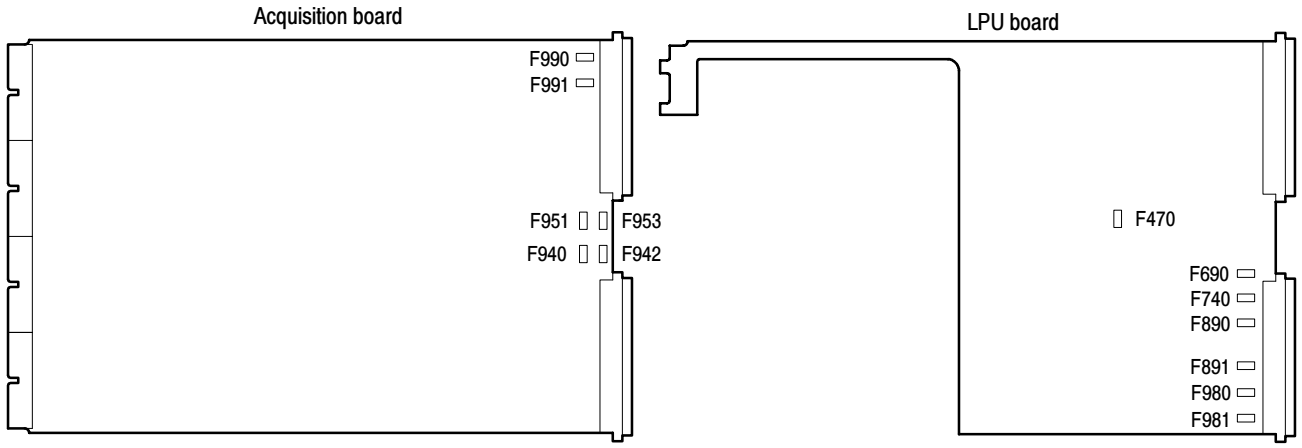

Figure 6-12: Fuse replacement

Installation

Use the following procedure and Figure 6-12 to install the fuses.

CAUTION. *To avoid damage to the module, use only replacement fuses that match the type, voltage, and current rating of the original fuse. Refer to Tables 6-4 and 6-5 on page 6-22 for the part number of replacement fuses.*

1. Solder the new fuse into place.
2. If you removed the Acquisition board, perform the *Acquisition Board* installation procedure (page 6-21).
3. Perform the *Local Processor Unit Board* installation procedure (see page 6-14).
4. Perform the *Cover* installation procedure (see page 6-8).

Rear EMI Gaskets

Removal

Use the following procedure and Figure 6-13 to remove the rear EMI gaskets.

1. Perform the *Cover* removal procedure (see page 6-7).
2. For the two rear gaskets on the chassis, perform the *Daughter Boards* removal procedure (page 6-11), the *Local Processor Unit Board* removal procedure (page 6-13), and the *Acquisition Board* removal procedure (page 6-17).
3. Lift the gasket fingers and rotate the gasket off (see Figure 6-13).

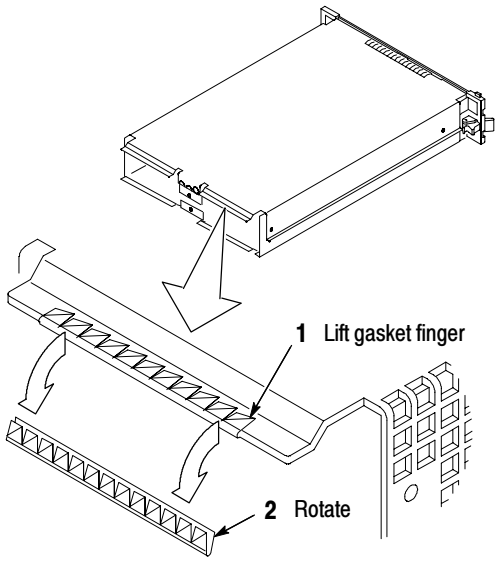

Figure 6-13: Rear EMI gasket removal

Installation

Use the following procedure and Figure 6–14 to install the rear EMI gaskets.

1. Position each gasket so the gasket fingers face the outside of the module.
2. Pick up each gasket at the end where the gasket finger is formed up. Then rotate the gasket on. As you do this, lift up any fingers that bind to the chassis or cover.
3. Slide each gasket gently from side to side to ensure that the gasket snaps in place.

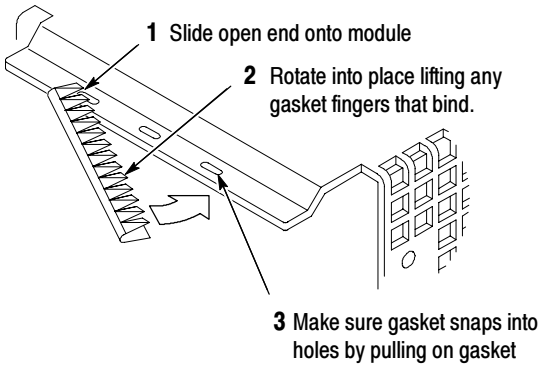

Figure 6-14: Rear EMI gasket replacement

4. Perform the *Acquisition Board* installation procedure (see page 6–21).

5. Perform the *Daughter Boards* installation procedure (see page 6–12).
6. Perform the installation procedure (see page 6–14).
7. Perform the *Cover* installation procedure (see page 6–8).

Troubleshooting

WARNING. *Before performing this or any other procedure in this manual, read the* General Safety Summary *and* Service Safety Summary *found at the beginning of this manual. Also, to prevent possible injury or damage to electrical components, read* Preventing Electrostatic Discharge *on page 6–1.*

This section contains information and procedures designed to help isolate faults to within the TLA7Nx, TLA7Px or TLA7Qx logic analyzer module. The process is as follows:

1. Review *Check for Common Problems*, beginning on page 6–28, to eliminate easy to find problems.
2. Perform procedures outlined in *Eliminate Other Problem Sources*, beginning on page 6–30, to eliminate the mainframe, probes, and other modules as the source of the fault(s).
3. Perform the *Troubleshoot the Logic Analyzer Module* procedure, beginning on page 6–31, to identify the failed replaceable part within the module.

If you replace a faulty circuit board or assembly found using these procedures, you must follow any verification and adjustment procedures identified in Table 6–8 on page 6–38 for the replaced board.

Service Level

This section supports isolation of faults within the logic analyzer module to the replaceable-part level that's reflected in the replaceable parts lists, which begin on page 10–2. In most cases, faults are isolated to circuit boards or assemblies, but not to individual components on those boards. (See *Strategy for Servicing* on page xv.)

Fault isolation is supported to the following circuit boards and replaceable parts:

- LPU board
- Acquisition board
- Daughter boards
- Power supply fuses
- Interconnect cables

Required Documentation

You may need to refer to additional TLA700 manuals to isolate faults. In addition, other manuals and other sections in this manual contain instructions you will need to complete repairs after locating a faulty part. For a list of supplimental documentation, refer to the following table.

Manual or Section	Purpose
TLA715 Portable Mainframe Service Manual or *TLA721 Benchtop Mainframe & TLA7XM Expansion Mainframe Service Manual*	To eliminate benchtop or portable mainframe as problem source (whichever configuration is in use).
Tektronix Logic Analyzer Family User Manual	To remove and reinstall modules in mainframe; to reinstall Windows 2000 or the TLA700 application software when required.
Removal and Installation Procedures (in this manual)	To remove and reinstall failed replaceable parts.
Replaceable Parts List (in this manual)	To order replaceable parts.

Check for Common Problems

Use Table 6–6 to quickly isolate possible failures. The table lists problems related to the logic analyzer module and possible causes. The list is not exhaustive, but it may help you eliminate a problem that's quick to fix, such as a blown fuse or loose cable.

Table 6-6: Failure symptoms and possible causes

Symptom	Possible cause(s)
Mainframe does not power on	■ Power connection faulty; check or substitute power cord ■ Fuse blown; check line fuse ■ Mainframe power supply failure; contact local Tektronix service center ■ Mainframe controller is not installed properly (or not at all)
Mainframe does not boot	■ Non-system disk or floppy in external drive; make sure logic analyzer boots from hard drive (Refer to the *Tektronix Logic Analyzer Family User Manual* for software reinstallation procedures) ■ Hard drive failure or corrupted files on hard drive; contact local Tektronix service center
Modules not recognized	■ Modules not fully inserted; make sure front of module is flush with front panel ■ Flash jumper installed on rear of module ■ Mainframe power supply failure; contact local Tektronix service center ■ Open fuses on logic analyzer module local processor unit board ■ Corrupted module firmware; reinstall firmware. Refer to the *Tektronix Logic Analyzer Family User Manual.*
Controller does not power on	■ Module not fully inserted; make sure front of module is flush with front panel ■ Module failure; contact local Tektronix service center
Module does not pass the normal power on diagnostics (READY indicator not green)	■ Module not fully inserted; make sure front of module is flush with front panel ■ Module failure; see *Troubleshoot the Logic Analyzer Module*, or contact local Tektronix service center ■ Open fuses on logic analyzer module local processor unit board or acquisition board
Module loses settings when power is turned off	■ Module failure; see *Troubleshoot the Logic Analyzer Module*, or contact local Tektronix service center ■ NV RAM failure; refer to page 6-13 for local processor unit board replacement instructions
Module will not acquire data or the acquired data is incorrect	■ Module failure; see *Troubleshoot the Logic Analyzer Module*, or contact local Tektronix service center ■ Faulty probe or leadset

Eliminate Other Problem Sources

The logic analyzer module is part of the TLA700 Series Logic Analyzer, which consists of modules installed in either the benchtop or portable mainframe. The following procedures will help you eliminate the mainframe and other modules as possible sources of the failure(s) that you troubleshoot.

Substitute a Good Module

If you have available a known-good logic analyzer module, perform the following procedure:

1. Remove the suspect logic analyzer module from the mainframe.
2. Install a known-good logic analyzer module in the same slot as the suspected module (verify that address switches on the rear of the module are set to same address as the module that you are replacing).
3. Power-on the logic analyzer and check for normal operation.
4. If the failure symptoms are still present with the known-good logic analyzer module installed, the problem most likely is in the portable mainframe or benchtop mainframe, not in the logic analyzer module.

NOTE. *Viewing the diagnostic window from the TLA700 logic analyzer application may help you isolate failures to individual modules or to the mainframe.*

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5. If the logic analyzer operates normally with the known-good logic analyzer module installed, the suspect logic analyzer module needs to be repaired. Refer to *Troubleshooting the Logic Analyzer Module* on page 6–31 for the troubleshooting procedures you need to locate faults.

Probe-Level Troubleshooting

If the fault is that the logic analyzer module acquires no data or faulty data, the probe may be at fault. Perform the following procedure to isolate such faults to a probe or to the logic analyzer module.

***NOTE**. The procedure below requires that the logic analyzer is functional and operates normally when the modules are installed. Procedures to functionally verify the probes are located in the probe manual.*

1. Verify that the probe is correctly connected to the module and to the system-under-test; check for loose or disconnected probe channels.
2. Move the suspected probe to another probe connector and observe if the problem follows the probe. If the problem does not follow the probe, the module may be faulty.
3. Substitute the suspected probe with a known good probe and observe if the problem is still present. If the problem still occurs, the module may be faulty. Refer to *Troubleshoot the Logic Analyzer Module* to isolate the problems within that module.
4. If you have determined that the probe is faulty, try to isolate the problem to an individual channel. A faulty channel may indicate a faulty probe podlet. Isolate faulty podlets by switching single podlets and observing if the problem tracks with the suspected podlet. Refer to the instructions in the probe manual for replacing faulty probe podlets.

Troubleshoot the Logic Analyzer Module

Follow the procedure in this section to identify the failed part within the logic analyzer module.

This procedure requires that the module is installed in a fully functional mainframe. If you have not determined that the mainframe is functional, or if you suspect the problem might be in a probe or in another module, refer to *Eliminating Other Problem Sources*.

Equipment Required

The basic troubleshooting procedures require minimal test equipment. There are no accessible test points to measure voltages. An ohmmeter is recommended for checking fuses.

Preparation

The fault isolation procedure requires that you:

- recognize codes flashed by the front-panel LEDs during power up
- are familiar with the power-on diagnostics

- know how to run extended diagnostics and self calibration

To fill these requirements, read the topics below before performing the *Fault Isolation Procedure* on page 6–33.

Calibration and Diagnostics Procedures

The following calibration and diagnostic procedures will help you diagnose problems.

Self Calibration. Use self calibration to calibrate the installed modules. Run the self calibration after a minimum of a 30 minute warm-up and prior to running the extended diagnostics. For more information on when to run the self calibration, refer to *Running the Self Calibration* on page 2–8.

Power-On Diagnostics. Power-on diagnostics check basic functionality of the logic analyzer at every power on. If any failures occur at power on, the screen displays the calibration and diagnostics property sheet.

If there are no diagnostic failures when you power on the logic analyzer, you can display and run the calibration and diagnostics property sheet by selecting Calibration and Diagnostics from the System menu.

Extended Diagnostics. The extended diagnostics execute more thorough tests than the power-on diagnostics. Using the extended diagnostics, you can do the following tasks:

- Run tests individually or as a group
- Run tests once or continuously
- Run tests until a failures occur

NOTE. *Certain diagnostic tests will fail if probes are attached. For best results, run the diagnostics with probes disconnected from the module.*

To run the extended diagnostics, do the following steps:

1. Disconnect probes from the module(s).
2. Start the TLA700 Series application if it is not already running.
3. From the System menu, select Calibration and Diagnostics.
4. Select the Extended Diagnostics property page.
5. Select the individual tests, group of tests, or all tests.
6. Click the Run button.

While the tests are executing, the word Running displays adjacent to the tests. When the tests are complete, either a Pass or Fail indication displays adjacent to each test.

Fault Isolation Procedure

The Primary Troubleshooting Tree (Figure 6–15 on page 6–35) provides troubleshooting steps that test the logic analyzer module. Use the following procedure with that tree.

To determine if module is recognized, perform the following steps:

1. Install the logic analyzer module into a known-good mainframe.
2. Before you power on the mainframe, look at the READY, ACCESSED ARM'D, and TRIG'D front panel indicators.
3. Power on the mainframe and note how the front panel indicators respond.
   a. Verify that the green READY indicator turns on while the diagnostics are being checked. If the green READY indicator does not turn on, the module is not being recognized which indicates possible problems on the Local Processor Unit board.
   b. Verify that after a few seconds the ACCESSED indicator turns on. The indicator stays on while the module is accessed by the controller. After the System window displays, the indicator blinks anytime the controller accesses the module.
4. If a and b are verified, the module is recognized; if not verified, the module is not recognized. Proceed as the troubleshooting tree instructs.
5. If diagnostic failures occur, replace the board indicated by the tree. For further confirmation, you can correlate the failed test displayed with a board using Table 6–7 on page 6–36. *You should also first check the "special cases" of diagnostic failures below:*
   - Note from the tree, that if all the diagnostics pass, but self calibration fails, replace the Acquisition board.
   - If any of the Kernel test groups fail (ROM check, LPU RAM, LPU Address decode, etc.) replace the LPU board.

- The At-Speed Threshold Acquire check tests the functionality of the daughter boards (TLA7N3, TLA7N4, TLA7P4 or TLA7Q4 only) and the Acquisition board. If this test fails for modules with daughter boards, and the DAC and both of the At-Speed Async Acquire pass, replace the daughter board; otherwise, replace the Acquisition board. Also, ensure that the probes are disconnected from the module before running the diagnostics.
- If multiple tests fail, the problem could be power-supply related problems on the Local Processor Unit board, faulty cables, or the mainframe. If replacing the Acquisition board does not remedy the failures, try replacing the Local Processor Unit board or the cables between the Local Processor Unit board and the Acquisition board.

NOTE*. Due to the module design, there are no accessible test points on the module to connect test equipment, such as an oscilloscope or digital voltmeter, to help isolate faults to an individual circuit board.*

6. Use the *Removal and Installation Procedures* that begin on page 6–5 to replace the faulty circuit board.

NOTE*. Before replacing modules, be sure to inspect all associated cables and connectors for damage and proper installation.*

7. Refer to Table 6–8 on page 6–38 after module replacement and perform *all* verification and adjustment procedures identified for the replaced module.

Primary Troubleshooting Chart

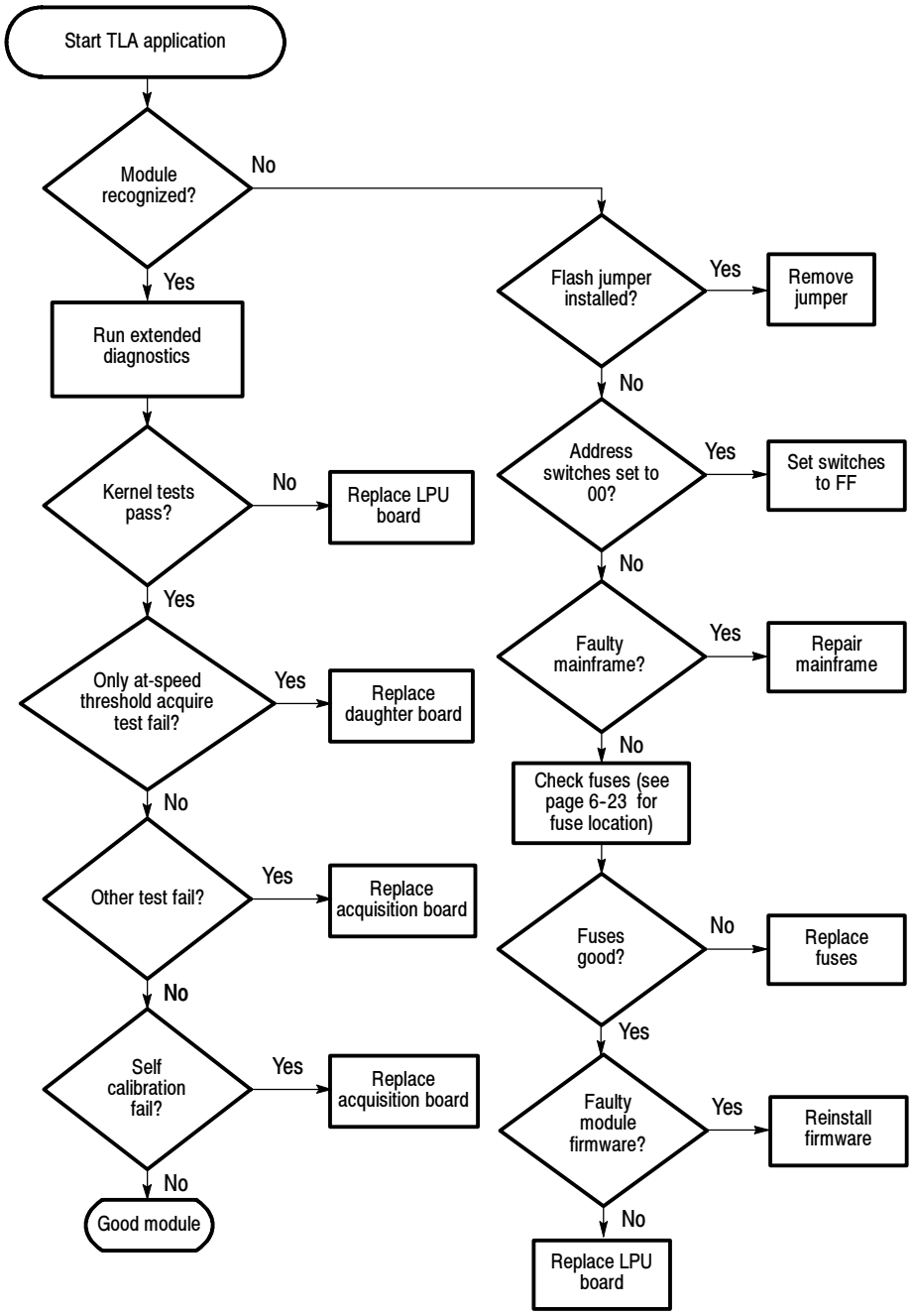

Figure 6-15: Primary troubleshooting chart

Diagnostic Tests Table

Table 6–7 can help you isolate problems to one of the three circuit boards in the module (use the *Removal and Installation Procedures* beginning on page 6–5 to replace the faulty circuit board):

Table 6-7: Diagnostic tests

Circuit board	Group & test	Power on	Extended
LPU board	Kernel		
	ROM Check	✓	✓
	LPU RAM	✓	✓
	Address Decode	✓	✓
	NVRAM Check	✓	✓
Acquisition board	Timestamp		
	Address/Data Bus	✓	✓
	Memory Address Rollover	✓	✓
	Timestamp Rollover	✓	✓
	Timestamp Fast Clock		✓
	Acquisition RAM Data Bus	✓	✓
	Acquisition RAM Address Bus	✓	✓
	Timestamp Acquire		✓
	Store Signals	✓	✓
Acquisition board	Clock		
	Address/Data Bus	✓	✓
	Qualifier/Combiner RAM	✓	✓
	Clock State Machine RAM	✓	✓
	MagniVu RAM	✓	✓
	Acquisition RAM Data Bus	✓	✓
	Acquisition RAM Address Bus	✓	✓
	Store Signals	✓	✓
	Flag Bus		✓
	Acquisition Data Path		
	Address/Data Bus	✓	✓
	MagniVu RAM	✓	✓
	Acquisition RAM Data Bus	✓	✓
	Acquisition RAM Address Bus	✓	✓
	Store Signals	✓	✓
	Bin & Log Busses	✓	✓

Table 6-7: Diagnostic tests (Cont.)

Circuit board	Group & test	Power on	Extended
Acquisition board	Trigger		
	Address/Data Bus	✓	✓
	Internal RAM	✓	✓
	Data Events		✓
	Clock Events		✓
	Log_G Signal	✓	✓
	Trigger Crossbar	✓	✓
	Signal/Trigger Lines	✓	✓
	Acquisition RAM		
	RAM Selection	✓	✓
	Acq/Clk/TS RAM		✓
	DAC	✓	✓
	Acquisition Address Decode	✓	✓
	At-speed Threshold Acquire[1]		✓
	At-speed Async Acquire		✓
	At-speed Sync Acquire		✓
Daughter board (TLA 7N3, TLA 7N4, TLA 7P3, and TLA 7P4 only)	Miscellaneous		
	At-speed Threshold Acquire[1,2]		✓

1 Ensure probes are disconnected before running this test.

2 Replace the daughter board if this test fails *and* both the DAC and the At-speed Async Acquire test pass.

Adjustment After Repair

After the removal and replacement of a circuit board or assembly due to electrical failure, locate the board removed in Table 6–8 and perform the indicated procedures.

Table 6-8: Requirements after replacement

Board replaced	Adjustment required	Verification checks
LPU board	Adjustment: Powerflex[1], Firmware level restoration[2], Deskew, Self Calibration	Self Calibration, Power-on and Extended Diagnostics
Acquisition board	Adjustment: Self Calibration, Deskew	Self Calibration, Power-on and Extended Diagnostics
Daughter boards	Adjustment: Deskew	Power-on and Extended Diagnostics

1 The PowerFlex restoration or changes can only be made by Tektronix service personnel.

2 Refer to the *Tektronix Logic Analyzer Family User Manual* for instructions for updating module firmware.

Overview of Procedures

Table 6–9 provides a brief overview of the troubleshooting, adjustment, verification, and calibration procedures.

***NOTE**. Calibration constants are stored in the LPU NVRAM. You must always perform a new self calibration and certification after you replace the LPU board.*

Table 6-9: Troubleshooting overview

Procedure	Recommended interval	Purpose	When required	Documented
Diagnostics (power on and extended)	Incoming inspection Annually	Verifies basic functionality.	During troubleshooting	*Power on Diagnostics*, page 6–32
Adjustment: self calibration	Annually As needed	Verifies basic functionality.	After acquisition, LPU, or daughter board replacement	*When to perform Self Calibration*, page 2–8
Adjustment: deskew	After board replacement or annually	Time-aligns the data channel	After board replacement	*Performance Verification* and *Adjustment Procedures*
Functional verification	Incoming inspection As needed	Verifies front end and basic functionality including probes	After board replacement	*Performance Verification* and *Adjustment Procedures*
Performance verification	Annually or as needed	Verifies advertised performance specifications	After board replacement	*Performance Verification* and *Adjustment Procedures*
Calibration (certification)	Annual recertification	Verifies primary references	After acquisition, LPU, or daughter board replacement	*Performance Verification* and *Adjustment Procedures*

Repackaging Instructions

This section contains the information needed to repackage the logic analyzer module for shipment or storage.

Packaging

If at all possible use the original packaging to ship or store the instrument. If the original packaging is not available, use a corrugated cardboard shipping carton having a test strength of at least 275 pounds (125 kg) and with an inside dimension at least six inches (15.25 cm) greater than the instrument dimensions. Add cushioning material to prevent the instrument from moving around in the shipping container. Seal the shipping carton with an industrial stapler or strapping tape.

Shipping to the Service Center

Contact the Service Center to get an RMA (return material authorization) number, and any return or shipping information you may need.

If the instrument is being shipped to a Tektronix Service Center, enclose the following information:

- The RMA number.
- The owner's address.
- Name and phone number of a contact person.
- Type of instrument and serial number.
- Reason for returning.
- A complete description of the service required.

***NOTE**. When ordering the LPU board for exchange or repair, you will need to supply the above information, including the firmware level and PowerFlex configuration information.*

Mark the address of the Tektronix Service Center and the return address on the shipping carton in two prominent locations.

CAUTION. *When returning the LPU board separately, be sure to properly support the narrow LED arm of the circuit board so it will not be damaged during transit or storage.*

Storage

The TLA7Nx, TLA7Px or TLA7Qx logic analyzer module should be stored in a clean, dry environment. The following environmental characteristics apply for both shipping and storage:

- Temperature range: -40° F to +160° F (-40° C to +71° C).
- Altitude: To 40,000 feet (12,190 meters).

See Table 1-9 on page 1-8 for a complete listing of the module environmental characteristics.

Options

This chapter lists the advertised options for each logic analyzer module. Refer to the *Mechanical Parts List* chapter for a list of standard and optional accessories for each module.

***NOTE**. Service options are listed on the Tektronix Service Options page that precedes the Table of Contents in this manual.*

TLA7N1, TLA7N2, TLA7N3 and TLA7N4 Options

Table 7–1 list options for the TLA7N1, TLA7N2, TLA7N3 and TLA7N4 modules. The number of probes per probe option depend on the number of channels in the logic analyzer module.

Table 7-1: TLA7N1, TLA7N2, TLA7N3 and TLA7N4 options

Option	Description
1S	256K @ 100 MHz
2S	1M @ 100 MHz
3S	4M @ 100 MHz
4S	64K @ 200 MHz
5S	256K @ 200 MHz
6S	1M @ 200 MHz
7S	4M @ 200 MHz
1P	P6418 Probe
2P	P6434 Probe
3P	P6417 Probe
D1	Add calibration data report

TLA7P2, TLA7P4, TLA7Q2 and TLA7Q4 Options

Table 7–2 list options for the TLA7P2 TLA7P4, TLA7Q2 and TLA7Q4 modules. The number of probes per probe option depend on the number of channels in the logic analyzer module.

Table 7-2: TLA7P2, TLA7P4, TLA7Q2 and TLA7Q4 options

Option	Description
1S	16M @ 200 MHz
D1	Add calibration data report
1P	P6418 Probe
2P	P6434 Probe
3P	P6417 Probe

Service Options

Tektronix offers the following service options.

Product installation service[1]	Option IN	Provides initial product installation/configuration and start-up training session including front panel and product familiarization.
Three years of calibration services	Option C3	Provides factory calibration certification on delivery, plus two more years of calibration coverage. Throughout the coverage period the instrument will be calibrated according to its Recommended Calibration Interval.
Test data	Option D1	Provides initial Test Data Report from factory on delivery.
Test data	Option D3	Provides test data on delivery plus a Test Data Report for every calibration performed during 3 years of coverage – requires Option C3.
Three years repair coverage	Option R3	Extends product repair warranty to a total of three years.

1 Availability of installation and on-site services depends on the type of product and may vary by geography.

Tektronix Service Options are available at the time you order your instrument. Contact your local Tektronix Sales Office for more information.

Electrical Parts List

Refer to the *Mechanical Parts List* section for a complete listing and description of replaceable parts.

Diagrams

Interconnection Block Diagram

This chapter contains the block diagram and the interconnection diagram for the logic analyzer module.

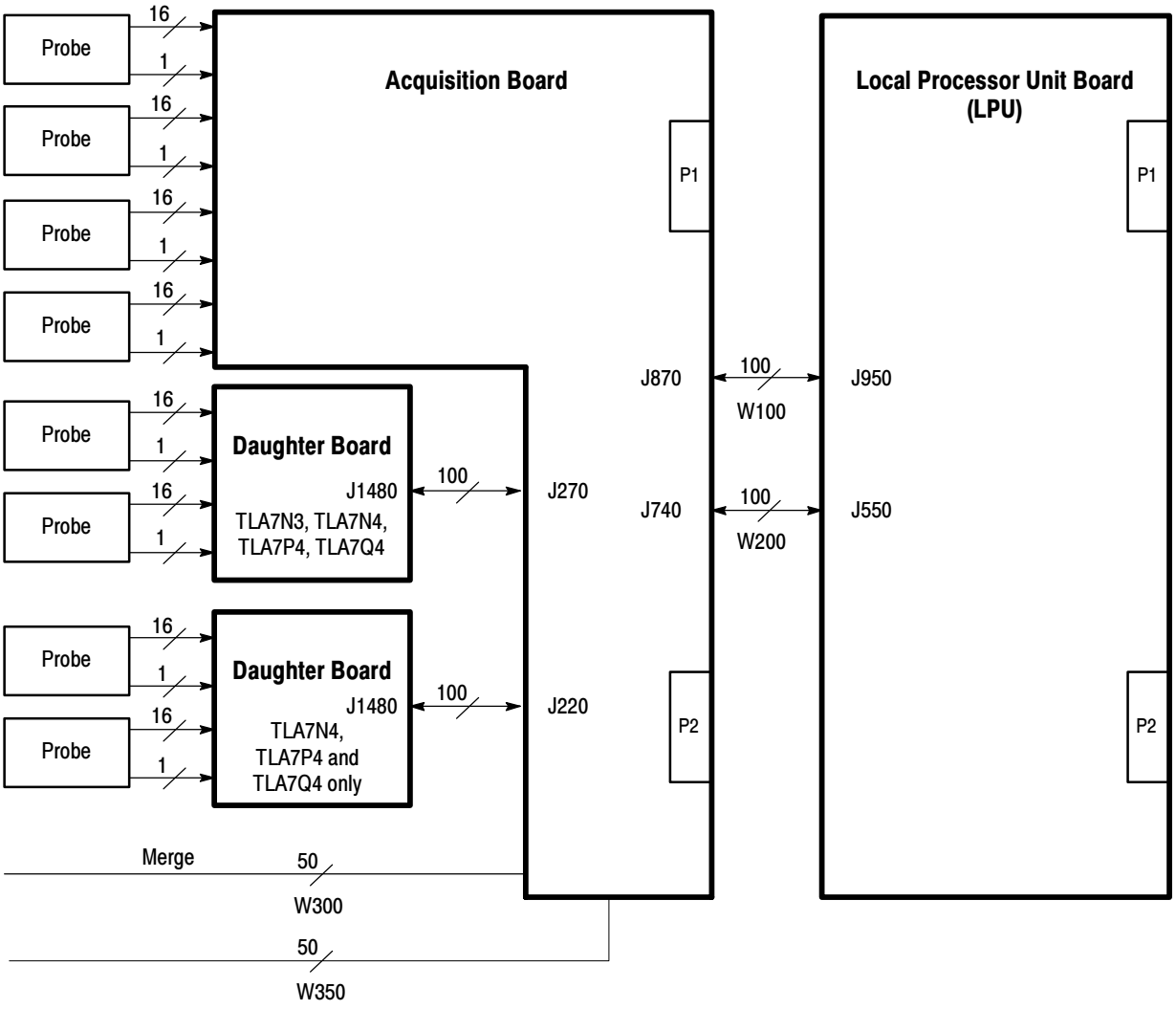

Figure 9-1: Interconnections

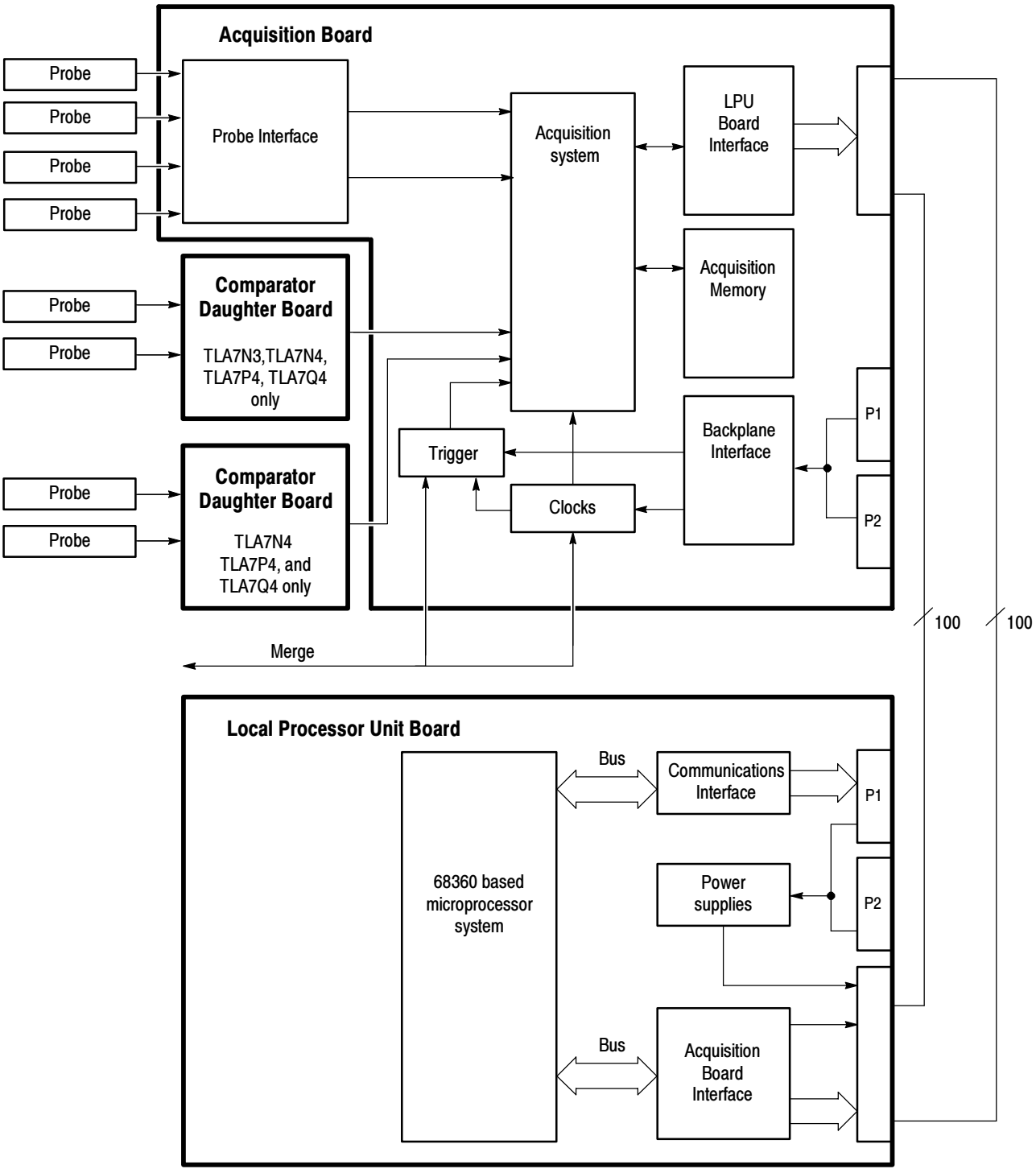

Figure 9-2: Block diagram

Mechanical Parts List

This section contains a list of the replaceable parts for the TLA7Nx, TLA7Px and the TLA7Qx logic analyzer modules. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

When you exchange some circuit boards, such as the local procession unit (LPU) board, you must supply the following information. This will allow the board to be preconfigured to the proper PowerFlex level for your logic analyzer. Alternatively, you can return the repaired module (with the necessary information) to your local service center for configuration.

- Model number
- Serial number
- PowerFlex option upgrade number
- Firmware level

Module Servicing

Modules can be serviced by selecting one of the following three options. Contact your local Tektronix service center or representative for repair assistance.

Module Exchange

In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-833-9200 and choose option 2.

New Modules

You may purchase replacement modules in the same way as other replacement parts.

Using the Replaceable Parts List

This section contains a list of the mechanical and/or electrical components that are replaceable for the instrument. Use this list to identify and order replacement parts. The following table describes each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section reference figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	TYCO ELECTRONICS	CUSTOMER SERVICE DEPT, PO BOX 3608	HARRISBURG, PA 17105-3608
05820	EG & G WAKEFIELD	60 AUDUBON ROAD	WAKEFIELD, MA 01880
060D9	TENSOLITE COMPANY	PRECISION HARNESS AND ASSEMBLY 3000 COLUMBIA HOUSE BLVD #120	VANCOUVER, WA 98661
06090	RAYCHEM CORP	300 CONSTITUTION DR	MENLO PARK, CA 94025-1111
06383	PANDUIT CORP	17303 RIDGELAND AVE	TINLEY PARK, IL 60477-3048
0JR05	TRIQUEST PRECISION PLASTICS	3000 LEWIS & CLARK HWY, PO BOX 66008	VANCOUVER, WA 98666-6008
0GV90	GLOBTEK INC	186 VETERANS DRIVE	NORTHVALE, NJ 07647-2303
0KB01	STAUFFER SUPPLY CO	810 SE SHERMAN	PORTLAND, OR 97214-4657
0KB05	NORTH STAR NAMEPLATE INC	5750 NE MOORE COURT	HILLSBORO, OR 97124-6474
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG, MD 20879
13103	THERMALLOY INC	2021 W. VALLEY VIEW LN, PO BOX 810839	DALLAS, TX 75381-5381
18677	SCANBE CORP	A ZERO CORP COMPANY, 3445 FLETCHER AVE	EL MONTE, CA 91731
22526	BERG ELECTRONICS INC	825 OLD TRAIL ROAD	ETTERS, PA 17319
23633	RICHEY ELECTRONICS INC	7441 LINCOLN WAY	GARDEN GROVE, CA 92641
26742	METHODE ELECTRONICS INC	BACKPLAIN DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656-4548
50434	HEWLETT PACKARD	370 W TRIMBLE ROAD	SAN JOSE, CA 95131-1008
53387	3M COMPANY	ELECTRONICS PRODUCTS DIV 3M AUSTIN CENTER	AUSTIN, TX 78769-2963
55285	BERGQUIST COMPANY INC., THE	5300 EDINA INDUSTRIAL BLVD	MINNEAPOLIS, MN 55435-3707
55322	SAMTEC INC	810 PROGRESS BLVD, PO BOX 1147	NEW ALBANY, IN 47150
60381	PRECISION INTERCONNECT CORP.	16640 SW 72ND AVE	PORTLAND, OR 97224
61857	SAN-O INDUSTRIAL CORP	91-3 COLIN DRIVE	HOLBROOK, NY 11741
75915	LITTELFUSE INC	800 E NORTHWEST HWY	DES PLAINES, IL 60016-3049
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077-0001
81073	GRAYHILL INC	561 HILLGROVE AVE, PO BOX 10373	LAGRANGE, IL 60525
81312	WINCHESTER ELECTRONICS	DIV OF LITTON INDUSTRIES INC 400 PARK ROAD	WATERTOWN, CT 06795-0050
8X345	NORTHWEST SPRING MFG CO	5858 SW WILLOW LANE	LAKE OSWEGO, OR 97035
93907	CAMCAR DIV OF TEXTRON INC	ATTN: ALICIA SANFORD, 516 18TH AVE	ROCKFORD, IL 611045181
TK0198	AVNET INC	AVNET ELECTRONICS MKTG, AMERICA 15580 SW JAY STREET	BEAVERTON, OR 97006
TK1943	NEILSEN MANUFACTURING INC	3501 PORTLAND RD NE	SALEM, OR 97303
TK2449	SINGATRON ENTERPRISE CO LTD	13925 MAGNOLIA AVE	CHINO, CA 91710
TK2469	UNITREK CORPORATION	3000 LEWIS & CLARK HWY SUITE 2	VANCOUVER, WA 98661
TK2647	INSTRUMENT SPECIALTIES CO INC.	C/O TEMCO NW, 1336 SE 51ST STREET	HILLSBORO, OR 97123

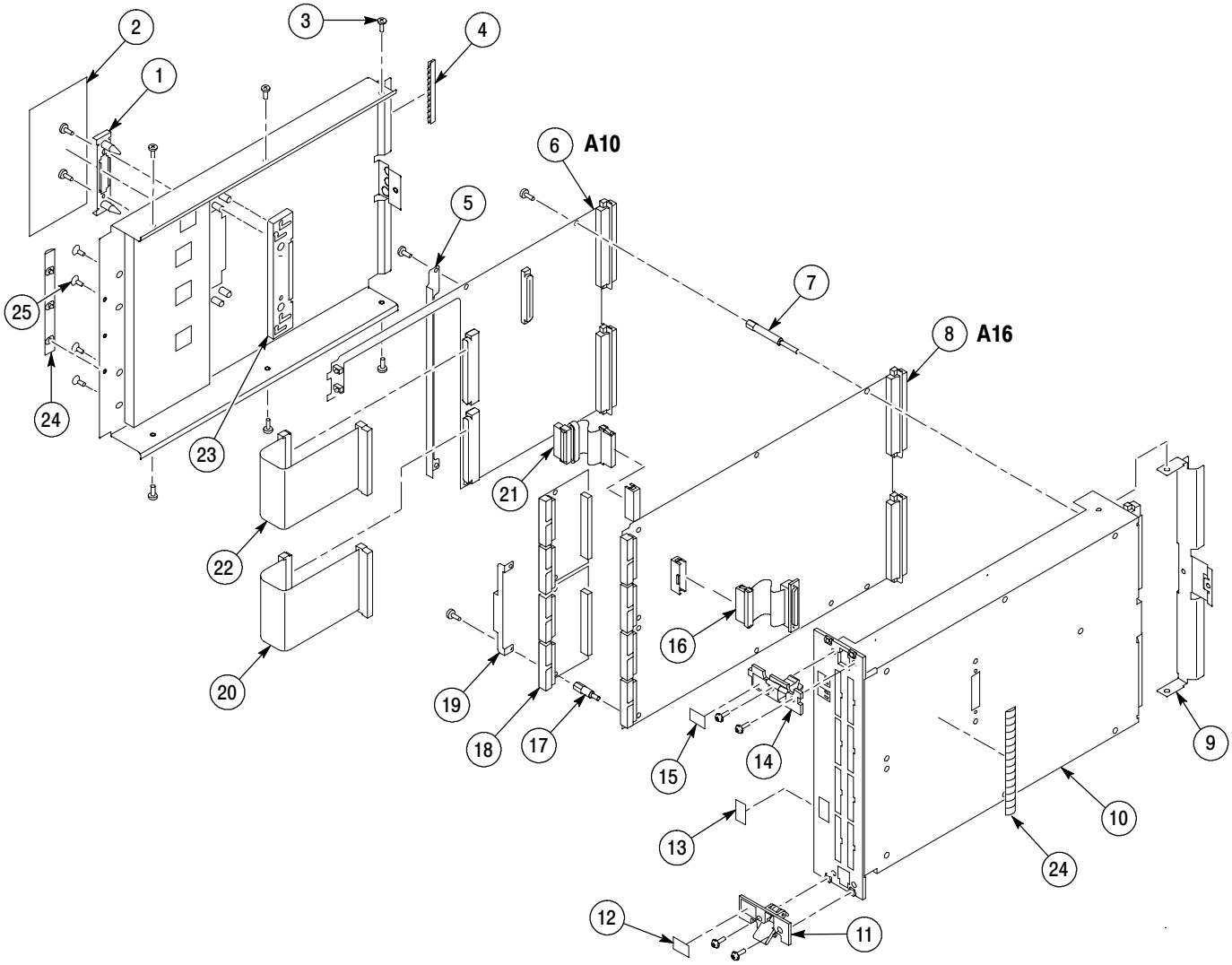

Figure 10-1: TLA700 Series Logic Analyzer Module exploded view

TLA700 Series module replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1-1	407-4458-XX			1	BRACKET,CABLE;TLA7N3/7N4/7P4/7Q4 MALE MERGE ASSEMBLY	80009	407-4458-XX
1-2	200-4338-XX			1	COVER:HOLE COVER FOR TLA7N1/7N2/7P2/7Q2 NON-MERGED MODULES	0KB05	ORDER BY DESCR
1-3	211-0409-XX			27	TLA7N1/7N2 SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,CDPL,T-10 TORX	0KB01	211-0409-XX
				29	TLA7N3/7N4 SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,CDPL,T-10 TORX	0KB01	211-0409-XX
				17	TLA7P2/7Q2 SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,CDPL,T-10 TORX	0KB01	211-0409-XX
				25	TLA7P4/7Q4 SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,CDPL,T-10 TORX	0KB01	211-0409-XX
1-4	348-1537-XX			4	TLA7N3/7N4/7P4/7Q4 GASKET,EMI:CLIP-ON,1.98 L, BE CU,TIN PLATED,W/T LANCES	0KB01	211-0409-XX
1-5	407-4489-XX			1	BRACKET, LPU BUS CABLES		
1-6	671-4252-XX			1	CKT BD ASSY: TLA7XX LPU, LOCAL PROCESSOR UNIT	80009	671-4252-XX
1-7	129-1478-XX			5	SPACER, POST:1.78 L,1.113 SPACING,W/0.35 L,0.25 HEX,W/4-40 INT THD X 6.32 EXTERNAL THD; NICKEL	80009	129-1478-XX
1-8	671-4214-XX			1	CIRCUIT BD ASSY:34 CH, 4M, 100MHZ TLA7N1 ACQUISITION	80009	671-4214-XX
	671-4215-XX			1	CIRCUIT BD ASSY:68 CH, 4M, 100MHZ TLA7N2 ACQUISITION	80009	671-4215-XX
	671-4216-XX			1	CIRCUIT BD ASSY:102 CH, 4M, 100MHZ TLA7N3 ACQUISITION	80009	671-4216-XX
	671-4217-XX			1	CIRCUIT BD ASSY:136 CH, 4M, 100MHZ TLA7N4 ACQUISITION	80009	671-4217-XX
	671-4238-XX			1	CIRCUIT BD ASSY:68 CH, 16M, 100MHZ TLA7P2 ACQUISITION	80009	671-4217-XX
	671-4239-XX			1	CIRCUIT BD ASSY:136 CH, 16M, 100MHZ TLA7P4 ACQUISITION	80009	671-4217-XX
	671-5332-XX			1	CIRCUIT BD ASSY:68 CH, 64M, TLA7Q2 ACQUISITION	80009	671-5332-XX
	671-5282-XX			1	CIRCUIT BD ASSY:136 CH, 64M, TLA7Q4 ACQUISITION	80009	671-5282-XX
1-9	386-6868-XX			1	BACK PANEL, TWO WIDE	TK1943	386-6868-XX
1-10	441-2155-XX			1	TLA7N1 CHASSIS ASSY: TWO WIDE, 34CH, W/SUB FRONT PANEL & LABEL ATTACHED	80009	441-2155-XX
	441-2156-XX			1	TLA7N2/7P2/7Q2 CHASSIS ASSY: TWO WIDE, 68CH, W/SUB FRONT PANEL & LABEL ATTACHED	80009	441-2156-XX
	441-2157-XX			1	TLA7N3 CHASSIS ASSY: TWO WIDE, 102CH, W/SUB FRONT PANEL & LABEL ATTACHED	80009	441-2158-XX
	441-2158-XX			1	TLA7N4/7P4/7Q4 CHASSIS ASSY: TWO WIDE, 136CH, W/SUB FRONT PANEL & LABEL ATTACHED	80009	441-2157-XX
1-11	367-0484-XX			1	HANDLE,EJECTOR:INJECTOR/EJECTOR ASSY, TWO WIDE,W/OUT KEYING,SPRING LOADED; PLASTIC	80009	367-0484-XX

TLA700 Series module replaceable parts list (Cont.)

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1-12	335-0646-XX			1	MARKER INDENT:EJECTOR LABEL,BOTTOM	0KB05	335064600
1-13	334-9636-XX			1	MARKER,IDENT:CONFIGURATION LABEL,MKD TLA7N1/7N2/7N3/7N4/7P2/7P4 TIMING,STATE SPEED,RAM DEPTH,0.010 POLY,GE LEXAN12 PER S	0KB05	334-9636-XX
	335-0451-XX			1	MARKER,IDENT:CONFIGURATION LABEL,MKD TLA7Q2/7Q4 TIMING,STATE SPEED,RAM DEPTH,0.010 POLY,GE LEXAN, 12 PER S	0KB05	335-0451-XX
1-14	367-0483-XX			1	HANDLE:INJECTOR/EJECTOR ASSEMBLY,TWO WIDE,W/KEYING,SPRING LOADED; PLASTIC	80009	367-0483-XX
1-15	334-9628-XX			1	MARKER,IDENT:LABEL,MKD TLA7N1,TOP INJECTOR/EJECTOR,0.010 POLY,GE LEXAN	0KB05	334-9628-XX
	334-9629-XX			1	MARKER,IDENT:LABEL,MKD TLA7N2,TOP INJECTOR/EJECTOR,0.010 POLY,GE LEXAN	0KB05	334-9629-XX
	334-9630-XX			1	MARKER,IDENT:LABEL,MKD TLA7N3,TOP INJECTOR/EJECTOR,0.010 POLY,GE LEXAN	0KB05	334-9630-XX
	334-9631-XX			1	MARKER,IDENT:LABEL,MKD TLA7N4,TOP INJECTOR/EJECTOR,0.010 POLY,GE LEXAN	0KB05	334-9631-XX
	334-9632-XX			1	MARKER,IDENT:LABEL,MKD TLA7P2,TOP INJECTOR/EJECTOR,0.010 POLY,GE LEXAN	0KB05	334-9632-XX
	334-9633-XX			1	MARKER,IDENT:LABEL,MKD TLA7P4,TOP INJECTOR/EJECTOR,0.010 POLY,GE LEXAN	0KB05	334-9633-XX
	335-0450-XX			1	MARKER,IDENT:LABEL,MKD TLA7Q4,TOP INJECTOR/EJECTOR,0.010 POLY,GE LEXAN	0KB05	335-0450-XX
	335-0449-XX			1	MARKER,IDENT:LABEL,MKD TLA7Q2,TOP INJECTOR/EJECTOR,0.010 POLY,GE LEXAN	0KB05	335-0449-XX
1-16	174-3537-XX			1	CA ASSY,SP:TLA7N3/7N4/7P4 MERGE RIBBON,IDC,30 AWG,0.025CTR,2.0 L	80009	174-3537-XX
1-17	129-1479-XX			4	SPACER, POST:1.135 OVERALL,0.510 L SPACING, W/0.35 L,0.25 HEX 4-40 INT THD X 6-32 EXT, 0.75 L	80009	129-1479-XX
1-18	671-3307-XX			1	TLA7N3 CKT BD ASSY:COMPARATOR DAUGHTER BD	80009	671-3307-XX
				2	TLA7N4/7P4/7Q4 CKT BD ASSY:COMPARATOR DAUGHTER BD	80009	671-3307-XX
1-19	407-4494-XX			1	TLA7N3/7N4/7P4/7Q4 BRACKET, EMI, DAUGHTER BD	80009	407-4494-XX
1-20	174-3949-XX			1	CA ASSY, SP, RIBBON; IDC, 100, 32 AWG, 0.025 CTR, 5.35 L, 2 FEMALE, RTANG 2 X 50, 0.05 X 0.1 CTR, RCPT, SYS50	060D9	174-3949-XX
1-21	174-3536-XX			1	CA ASSY, SP:TLA7N3/7N4/7P4/7Q4 MERGE RIBBON,IDC,30 AWG,0.025 CTR,2.5 L	80009	174-3536-XX
1-22	174-4378-XX			1	CA ASSY, SP, RIBBON; IDC, 100, 32 AWG, 0.025 CTR, 5.75 L, 2 FEMALE, RTANG 2 X 50, 0.05 X 0.1 CTR, RCPT, SYS50	TK2469	174-4378-XX
1-23	352-1062-XX			1	HOLDER,TLA7N3/7N4 MERGE:MALE, 18AWG CRS W/HARDWARE	TK1943	352-1062-XX

TLA700 Series module replaceable parts list (Cont.)

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1-24	335-0646-00			1	MARKER,IDENT:LABEL,MKD FOR USE WITH TLA700 SERIES,BOTTOM INJECTOR/EJECTOR,0.745 X 0.520,0.010	0KB05	335-0646-00
				2	TLA7N3/7N4/7P4/7Q4 SHLD GSKT,ELEC:SYMETRICAL SLOTTED FINGER,0.350 W X 7.5 L,RIVIT MTG,SNAP-IN,RIVIT SPACING 1.5 IN	TK2647	0493-0069-XX
1-25	211-0718-XX			4	TLA7N3/7N4/7P4/7Q4 SCREW,MACHINE;6-32 X 0.312,FLH100,STL,CDPL,T-10 TORX	0KB01	ORDER BY DESCR
					OPTIONAL ACCESSORIES		
-	071-0912-XX			1	MANUAL, TECH: SERVICE, TLA721 BENCHTOP & TLA7XM EXPANSION MAINFRAME	80009	071-0912-XX
-	071-0913-XX			1	MANUAL, TECH: SERVICE, TLA715 PORTABLE MAINFRAME	80009	071-0913-XX
-	071-0865-XX			1	MANUAL, TECH: INSTRUCTION, TLA7UP MAINFRAME FIELD UPGRADE KIT	80009	071-0865-XX
-	071-0863-XX			1	MANUAL, TECH: USER, TLA SERIES	80009	071-0862-XX
-	071-0567-XX			1	MANUAL, TECH: P6417 & P6418 PROBE	80009	071-0567-XX
-	070-9793-XX			1	MANUAL, TECH: P6434 PROBE	80009	070-9793-XX
-	407-4435-XX			1	BRACKET,SUPPORT:PR0BE ASSY CLAMP,18 AWG STEEL, BLACK ANODIZE FINISH W/RETAINING WASHER	80009	407-4435-XX
-	174-3644-00			1	CA ASSY,SP:RIBBON,IDC,32 AWG,0.025 CTR,12.0 L,100 POS,MINIRIBBON,RCPT,CHAMP050 X 2 X 50,0.	060D9	174-3644-00
-	174-4331-00			1	CA ASSY,SP:RIBBON, IDC,32 AWG,0.025 CTR,7/40 STRAND,12L,80 POS 0.05 CTR,W/POLZ X 80 POS 0.0	060D9	174-4331-00

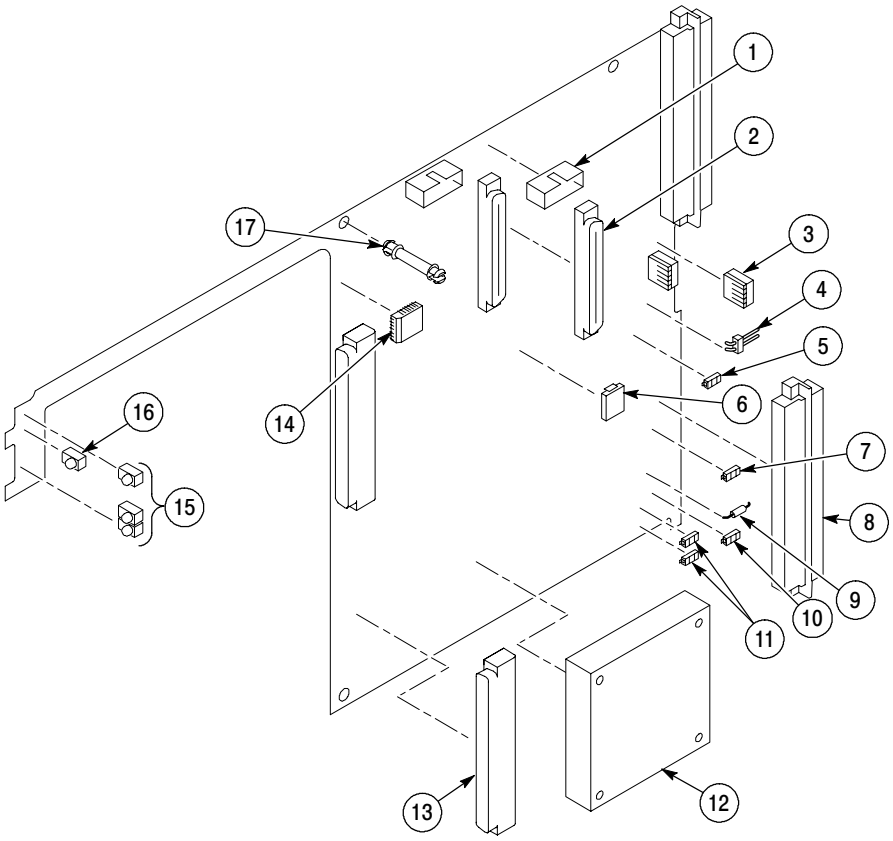

Figure 10-2: TLA700 Series LPU board exploded view

TLA700 Series LPU board replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2-1	131-3520-XX			2	CONN,HDR:TLA7N1/7N3/7N4/7P2/7P4/7Q2/7Q4 PCB,MALE,STR,2 X 5,0.1 CTR	53387	2510-6002UB
2-2	131-6576-XX			2	CONN,RIBBON:PCB,MALE,STR,80 POS,0.05 CTR, 0.391 H X 0.106 TAIL,30 GOLD,BRD LOCKS	00779	2-557102-1
2-3	260-2597-XX			2	SWITCH,ROTARY:HEXADECIMAL,100MA AT 50VDC,RIGHT ANGLE,0.430 W X 0.400 H X 0.202 L	81073	94HAB16RA
2-4	131-3766-XX			1	CONN,HDR:PCB,MALE,RTANG,1 X 2,0.1 CTR	00779	87232-2
2-5	159-5014-XX			1	TLA7N1/7N2 FUSE:2.0A,125V,FAST BLOW,0.1 X 0.1 X 0.24,UL REG,CSA CERT,	75915	R451 002
2-6	159-5008-XX			1	FUSE,THRM,CHIP:SELF RESETTING FUSE,1.5A HOLD,3.0A TRIP AT 20 DEG C,30V MAX,SMD150	06090	SMD150-2
2-7	159-5018-XX			1	TLA7N1/7N2 FUSE:3.0A,125V,FAST BLOW,0.1 X 0.1 X 0.24,UL REG,CSA CERT,T&R	75915	R451 003
2-8	131-3692-XX			2	RETENTION, HIGH TEMP, 94V-0; SAFETY CONTROLLED	00779	536416-5
2-9	159-0145-XX			1	FUSE,WIRE LEAD;15A,32V,10 SECONDS	61857	SP7-15A
2-10	159-5015-XX			1	TLA7N1/7N2 FUSE,SMD:10.0A,125V,FAST BLOW,0.1 X 0.1 X 0.24,UL REG,CSA CERT,	75915	R451 010
2-11	159-5009-XX			2	FUSE,SMD:1.5A,125V,FAST BLOW	75915	45101.5
2-12	119-5879-XX			1	POWER SUPPLY:99W,DC-DC,36-75V IN,3.3V 30A OUT,80% EFF,JW150F1,ECB MOUNT MODULE,	TK6073	JW150F1
2-13	131-6069-XX			2	CONN, RIBBON:PCB,MALE,RTANG,100 POS,0.05 CTR	00779	2-557100-5
2-14	163-1122-XX			1	TLA7N1/7N2 IC,DIGITAL:PRGM 156-6512-00:CMOS,PLD,EEPLD,22V10,7.5NS,140MA,22V10-7,PLCC28-1,TUBE	TK0198	163-1122-XX
2-15	150-1278-XX			3	DIODE,OPTO:LED,GRN,569NM,2MCD AT 5V	50434	HLMP-1640-010
2-16	150-1279-XX			1	DIODE,OPTO:LED,YEL,585NM,2MCD AT 5V	50434	HLMP-1620-010
2-17	386-1657-XX			4	SUPPORT,CKT BD:ACETY,RESIN NATURAL	0JR05	ORDER BY DESCR

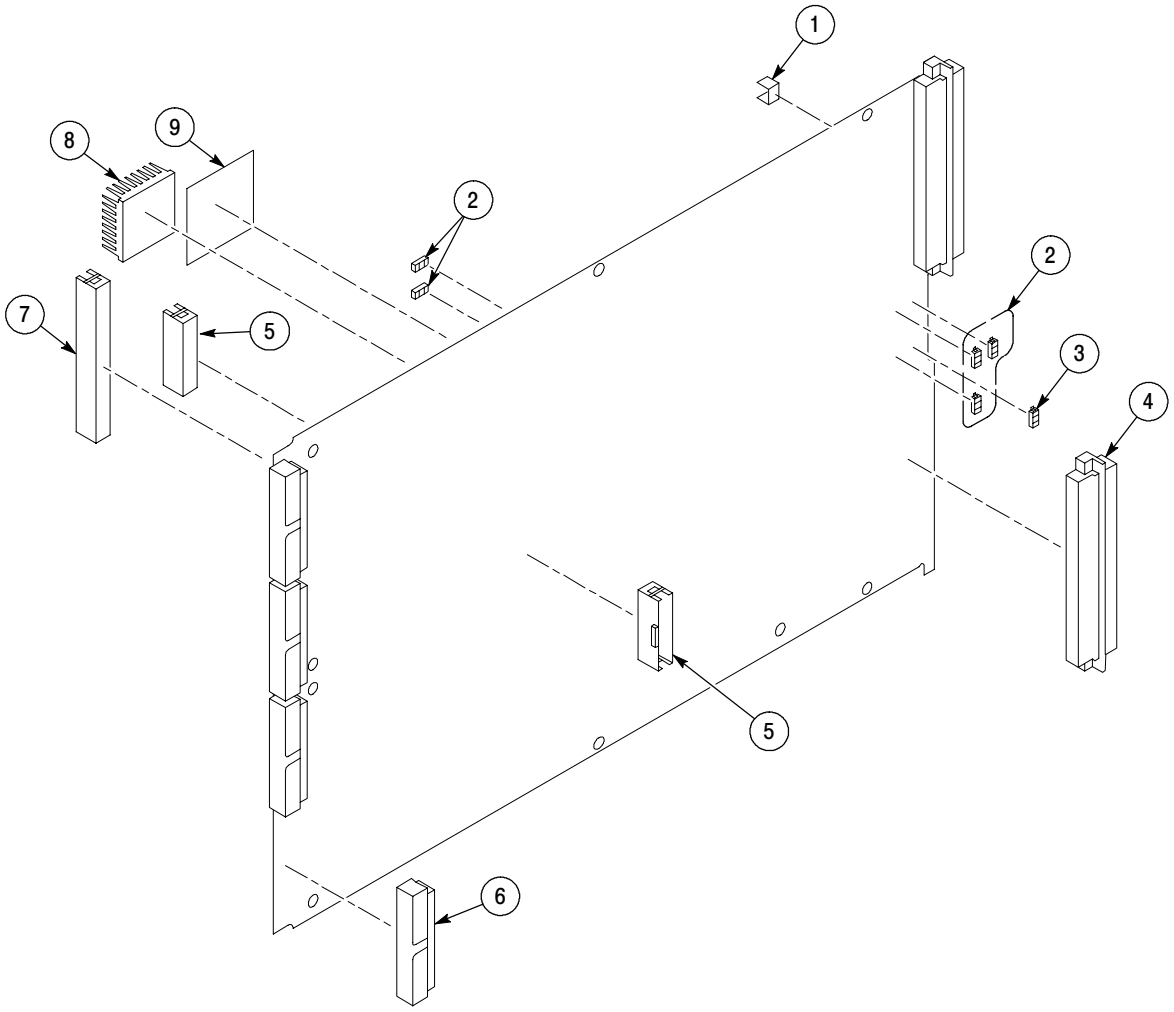

Figure 10-3: TLA700 Series Acquisition board exploded view

TLA700 series Acquisition board replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
3-1	131-6697-XX			1	CONN,HDR:SMD,MALE,STR,2 X 3, 0.079 CTR (2MM),0.232 H X 0.122 TAIL,30 GOLD	6D224	95615-106
3-2	159-5009-XX			5	FUSE,INLINE,SMD:1.5A,125V,FAST BLOW	75915	45101.5
	159-0159-XX			5	FUSE,THRU-HOLE (REPLACEMENT) SMD:1.5A,125V,FAST BLOW	75915	25101.5
3-3	159-5010-XX			1	FUSE,INLINE,SMD:7A,125V,FAST BLOW	75915	451007
	159-0146-XX			1	FUSE,THRU-HOLE (REPLACEMENT) SMD:7A,125V,FAST BLOW	75915	251007
3-4	131-6174-XX			2	CONN,DIN:PRESSFIT,MALE,RTANG,3 X 32,0.1 CTR	81312	96P603307319
3-5	131-6021-XX			2	TLA7N3/7N4/7P4/7Q4 CONN,HDR:SMD,MALE,STR,2 X 25, 0.05 X 0.1 CTR,0.480 H, SHRD/4 SIDES, CTR PLZ, LATCHING, W/O BDRETENTION,30 GOLD	00779	146144-3
3-6	131-3363-XX			4	TLA7N2/7N3/7N4/7P2/7P4/7Q2/7Q4 CONN,HDR:PCB,MALE, RTANG,2 X 17,0.1CTR	53387	N2534-5002UB
				2	TLA7N1 CONN,HDR:PCB,MALE,RTANG,2 X 17,0.1CTR	53387	N2534-5002UB
3-7	131-5980-XX			4	TLA7N4/7P4/7Q4 CONN,HDR:SMD,MALE,STR,2 X 50,0.05 X 0.1 CTR	00779	1-104549-0
				2	TLA7N1/7N2/7P2/7Q2 CONN,HDR:SMD,MALE,STR,2 X 50,0.05 X 0.1 CTR	00779	1-104549-0
				1	TLA7N3 CONN,HDR:SMD,MALE,STR,2 X 50,0.05 X 0.1 CTR	00779	1-104549-0
3-8	214-4747-XX			2	TLA7N1 HEAT SINK,SEMIC:IC,PGA 11X11/MQUAD,1.1" X 1.1" X 0.45" H,PIN FIN,ALUMINUM,BLACK	05820	658-45AB
				3	TLA7N2/7P2/7Q2 HEAT SINK,SEMIC:IC,PGA 11X11/MQUAD, 1.1" X 1.1" X 0.45" H,PIN FIN,ALUMINUM,BLACK	05820	658-45AB
				4	TLA7N3 HEAT SINK,SEMIC:IC,PGA 11X11/MQUAD,1.1" X 1.1" X 0.45" H,PIN FIN,ALUMINUM,BLACK	05820	658-45AB
				5	TLA7P4/7Q4/7N4 HEAT SINK,SEMIC:IC,PGA 11X11/MQUAD,1.1" X 1.1" X 0.45" H,PIN FIN,ALUMINUM,BLACK	05820	658-45AB
3-9	214-4748-XX			2	HEAT SINK,SEMIC:IC,PGA 11X11/MQUAD,1.1" X 1.1" X 0.25" H,PIN FIN,ALUMINUM,BLACK	05820	658-25AB

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					ADJUSTMENT/VERIFICATION FIXTURE		
10-4-1	131-5267-00			1	CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR	00779	104326-4
-2	131-5829-00			1	CONN,SHUNT:JUMPER,FEMALE,STR,1 EA,2MM,4MM H,	00779	382575-3
-3	131-5990-00			1	CONN,HDR:PCB,MALE,STR,1 X 36,0.079 CTR	55322	TMM-136-02-G-2
-4	131-0608-00			5	CONN,TERMINAL:PRESSFIT/PCB,MALE,STR,0.025 SQ,0.248 MLG X 0.137 TAIL,50 GOLD,PHZ BRZ,W/FERRULE	22526	48283-018
-5	131-6024-00			1	CONN,HDR:PCB,MALE,STR,2 X 25,0.079CTR	53387	151250-8422-TY
-6	105-1089-00			2	LATCH ASSY:LATCH HOUSING ASSY,VERTICAL MOUNT,2/PKG,0.48 H X 1.24 L,W/PCB SINGLE CLIP	60381	105-1089-00
-7	131-6134-01			2	CONN,PLUG:SMD,MICTOR,PCB,FEMALE	00779	767004-1
-8	210-0457-00			6	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL,W/LOCKWASHER	0KB01	ORDER BY DESCR
-9	348-0048-00			6	FOOT,CAMERA:BLACK VINYL W/6-32 STUD	80009	348-0048-00
-10	210-0586-00			4	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	0KB01	ORDER BY DESCR
-11	671-3599-01			1	CKT BD ASSY:DESKEW TEST FIXTURE (A14)	80009	671-3599-01
-12	150-5009-00			1	DIODE,OPTO:LED,HI-EFFIC RED,626NM,3.4MCD AT 10MA	50434	HLMP-6305-021
-13	159-5009-00			1	FUSE,SMD:1.5A,125V,FAST BLOW,0.1 X 0.1 X 0.24,UL RECOGNIZED,CSA CERTIFIED	75915	45101.5
-14	131-5527-00			1	JACK,POWER DC:PCB,MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWI	TK2449	DJ-005-A
-15	214-2957-00			2	HEAT SINK,SEMIC:TRANSISTOR,TO-220	13103	6072B
-16	210-1178-00			2	WASHER,SHLDR:TRANSISTOR,TO-220,0.2"ODX0.116	13103	7721-7PPS
-17	211-0372-00			4	SCREW,MACHINE:4-40 X 0.312,PNH,STL CD PL,TORX T10	93907	B80-00020-003
-18	342-0355-00			2	INSULATOR,PLATE:TRANSISTOR,SILICONE RUBBER	55285	7403-09FR-51
-19	131-3378-00			2	CONN,RF JACK:BNC,50 OHM,FEMALE,RTANG,PCB/REAR PNL,0.5-28 THD,0.625 H X 0.187 TAIL,W/O MTG FL	00779	227677-1
	119-4855-00			1	POWER SUPPLY:EXTERNAL,WALL MOUNT,18W,120VAC 60HZ IN,12VDC 1.5A OUT,UNREG,USA,183CM CABLE,STR	0GV90	WD1E1500C12CP
	119-4856-00			1	POWER SUPPLY:EXTERNAL,WALL MOUNT,18W,220VAC 50HZ IN,12VDC 1.5A OUT,UNREG,EUROPEAN,183CM CABLE	0GV90	WD13E1500C12CP
	119-4857-00			1	POWER SUPPLY:EXTERNAL,WALL MOUNT,18W,220VAC 50HZ IN,12VDC 1.5A OUT,UNREG,UK,183CM CABLE,STR C	0GV90	WD35E1500C12CP
	119-4859-00			1	POWER SUPPLY:EXTERNAL,WALL MOUNT,18W,100VAC 60HZ IN,12VDC 1.5A OUT,UNREG,JAPAN,183CM CABLE,ST	0GV90	WD49E1500C12CP

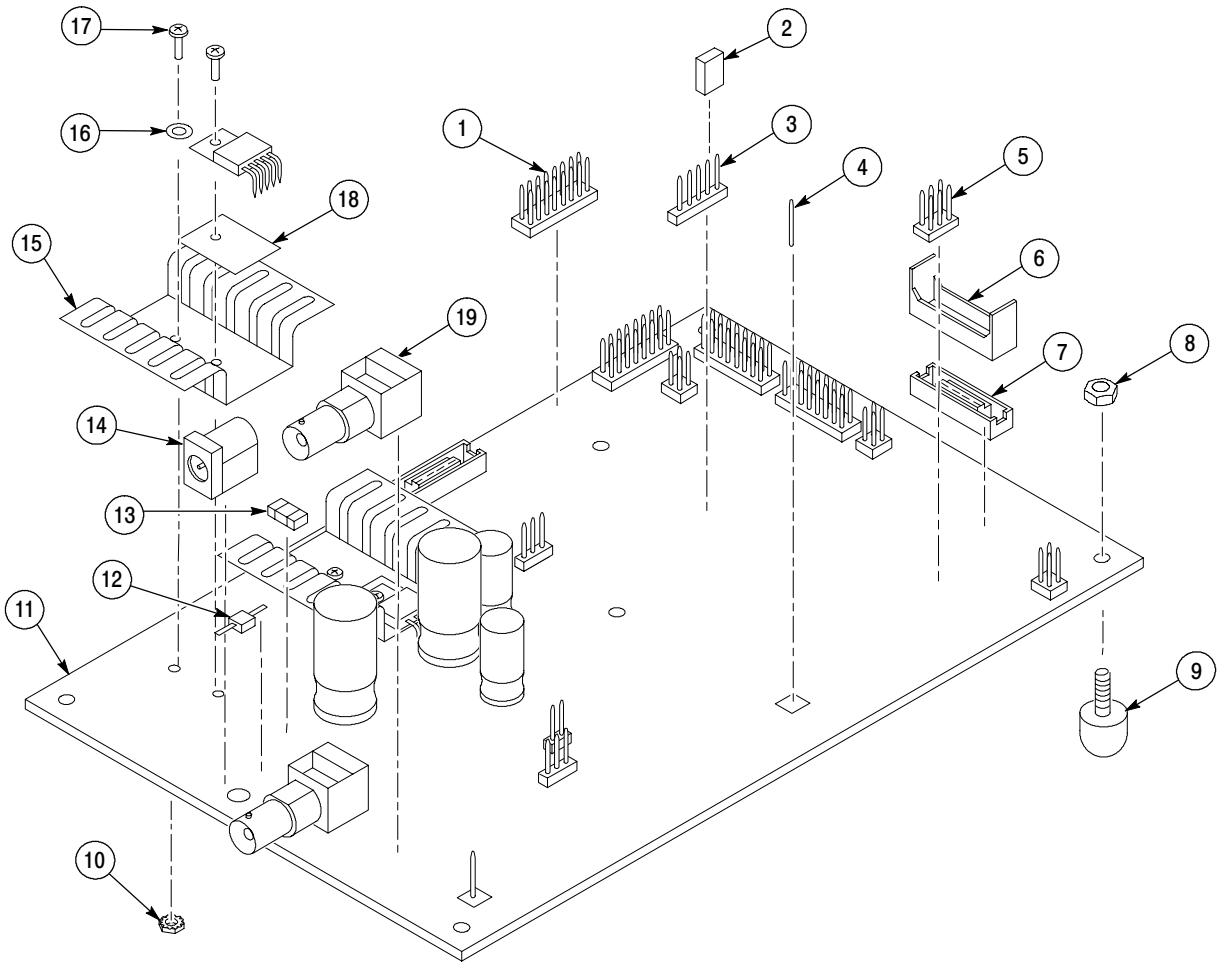

Figure 10- 4: Adjustment/verification fixture exploded view